



LIGHTWAVE LOGIC™

Faster by Design

PIC Pilot Lines: Competitive Positioning

Michael Lebby

8th November 2021

PIC International: PIC Pilot Line Keynote

The information in this presentation may contain forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995. You can identify these statements by use of the words "may," "will," "should," "plans," "explores," "expects," "anticipates," "continue," "estimate," "project," "intend," and similar expressions. Forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those projected or anticipated. These risks and uncertainties include, but are not limited to, general economic and business conditions, effects of continued geopolitical unrest and regional conflicts, competition, changes in technology and methods of marketing, delays in completing various engineering and manufacturing programs, changes in customer order patterns, changes in product mix, continued success in technological advances and delivering technological innovations, shortages in components, production delays due to performance quality issues with outsourced components, and various other factors beyond the Company's control.

This orange bar is the takeaway summary from each slide...

Slides will be posted at:
www.lightwavelogic.com and <https://picpilotlines.net>

The screenshot shows the Lightwave Logic website homepage. At the top, there is a navigation bar with links for 'ABOUT US', 'TECHNOLOGY', 'RESOURCE CENTER', 'INVESTORS', and 'CONTACT US'. The main header features a large image of fiber optic cables with the text 'Creating Solutions For Moving More Data. Faster, Easier And Simpler'. Below this, there are two columns: 'Corporate Video' on the left, which includes a video player for 'Lightwave Logic | Internet throughput maximization', and 'News & Events' on the right, which lists several news items with dates and titles.

The screenshot shows the agenda page for the PIC Pilot Lines Conference. The page is titled 'AGENDA' and lists the schedule for Monday 8th November 2021 starting at 14:00 BST. The agenda includes various sessions such as 'Registration', 'Opening remarks from Michael Leiby & Jose Pazo', 'Setting up a legal and IP framework for photonics consortiums and SMEs', 'Platform Partner Presentation 1 - Photonics Manufacturing and Pilot Lines in the Era of the Coronavirus', 'JAPPIE', 'MedPub', 'Med II Alliance (formerly MEDPHAD)', 'PICPilotQ Pilot Line for fine form micro-optics and in a one-stop shop for SMEs up to LMEs', 'PICAPP', 'PICPilot Pilot Line - The world's premier SMF pilot line for integrated biophotonic applications', 'ePHO4 - The European Silicon Photonics Alliance', 'Coffee Break', 'Platform Partner Presentation 2 - Two-photon grayscale lithography for wafer-level optics and photonic packaging', 'User Presentation 1 - Possibilities of Backflow silicon nitride', 'Lundia Photonics', 'Keynote - Presentation title TBD', 'Keynote - PICing silicon? European photonics and PIC pilot lines - a success story', 'Closing Remarks by Michael Leiby & Jose Pazo', and 'Pre-Conference Networking Reception, open to all PIC Pilot Lines Attendees'.

Sit back...relax (no need to take notes!)

- **Can the PIC pilot lines provide product value?**
- **Can we integrate the PIC pilot lines into a competitive infrastructure environment?**
- **What's needed to make sure our PIC infrastructure is successful in manufacturing over the next decade?**

What might be the impact of PICs over the next decade?

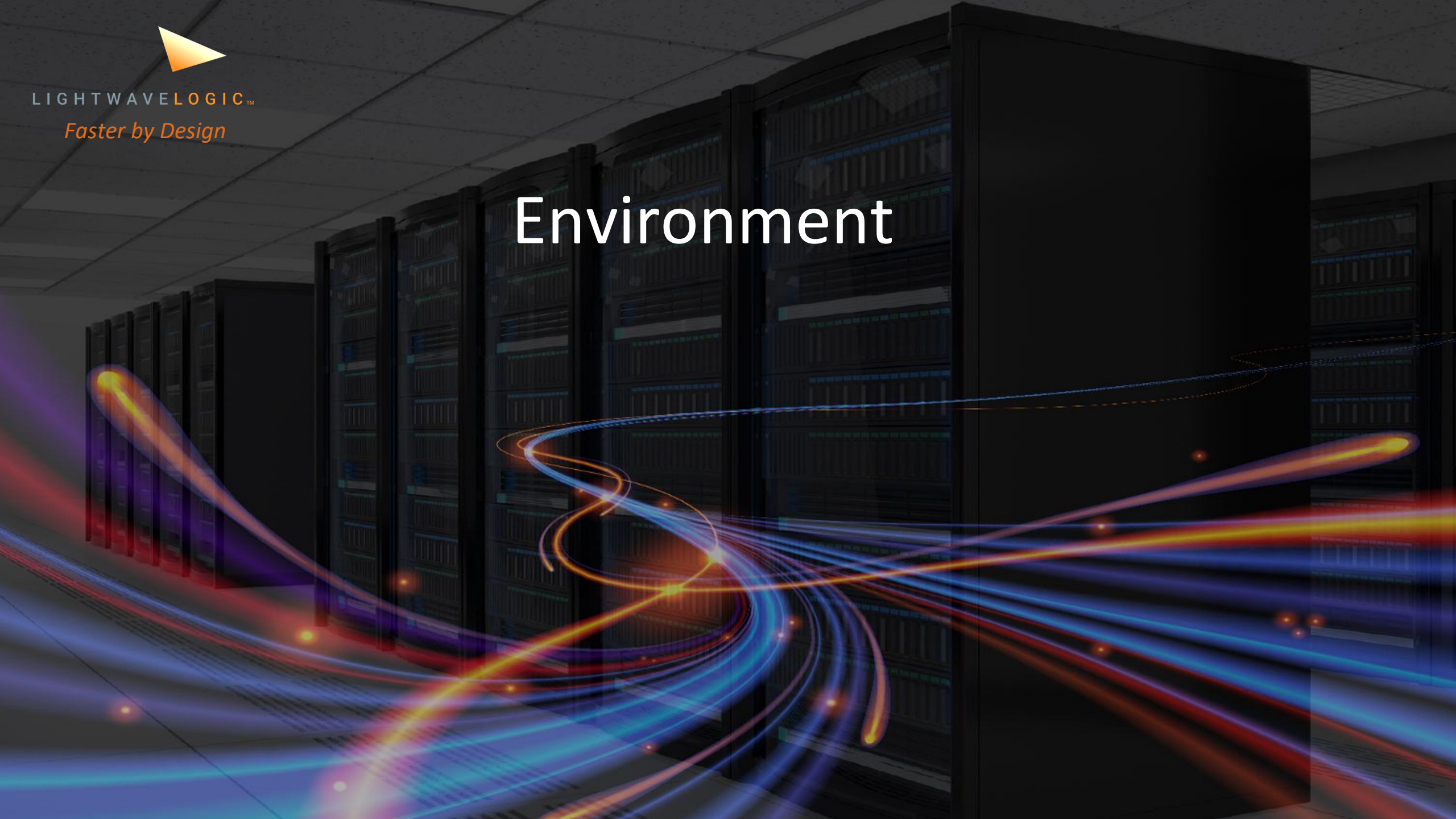
- ❑ Environment
- ❑ Pilot Lines
- ❑ Roadmaps
- ❑ Creating a PIC infrastructure
- ❑ Summary



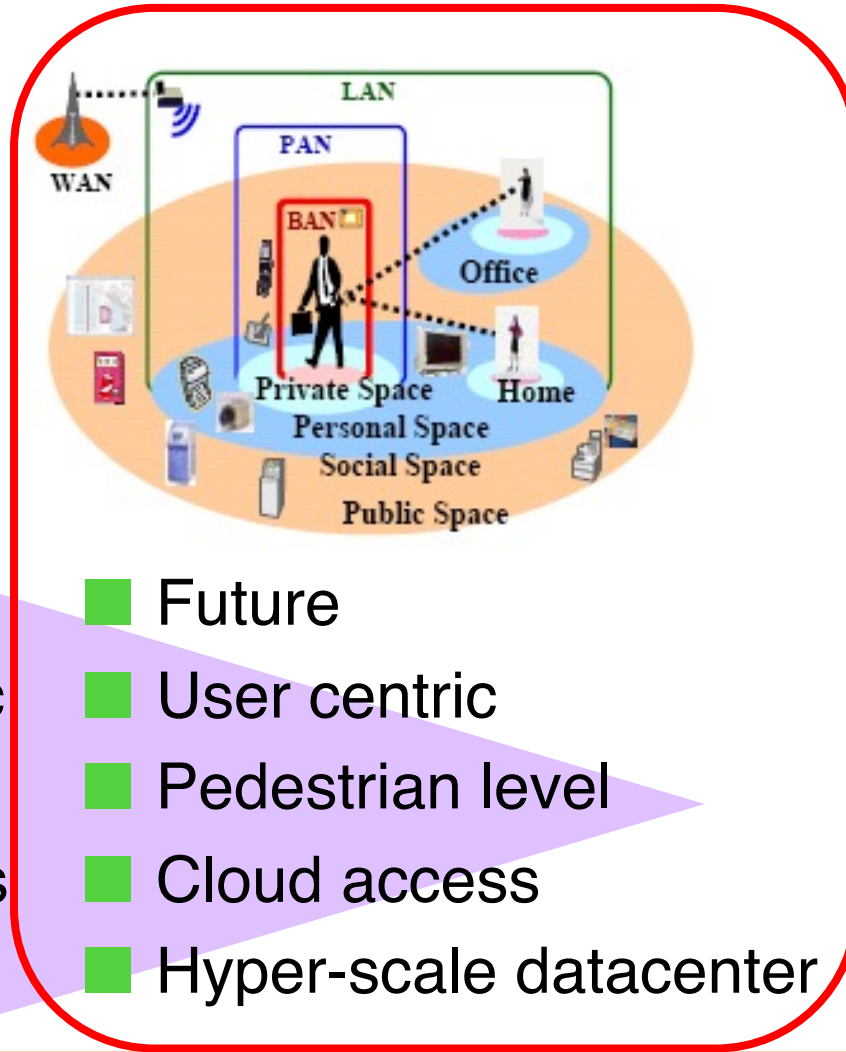
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Environment



Photonics as a catalyst for change in lifestyle...



- Before
- Computer centric
- Experts level
- Data exchange
- Exchange

- Today
- Network centric
- Trained level
- Archival access
- Datacenter

- Future
- User centric
- Pedestrian level
- Cloud access
- Hyper-scale datacenter

Use of photonics

Use of data...

Use of displays

Use of lighting...

Lifestyle evolves towards personal space...

Photonics markets broaden significantly

Photonics applications	Photonics → 2030 (rough forecasts*)	Opportunity for PICs (polymer & silicon photonics/InP)
5G systems/back haul/RF	~\$4-10B	Existing
Display/project	~\$5-20B	Yes
Automotive (LIDAR)	~\$20-50B	Yes
Optical sensing/3D	~\$2-5B	Yes
Bio-photonic sensing	~\$2-5B	Yes
Medical	~\$5-10B	Yes
Instrumentation	~\$1-3B	Yes
Fiber comms	~\$40-60B	Existing
HPC/computational/AI	~\$10-20B	Existing
DCI/datacenter	~\$20-30B	Existing

Photonics, and PICs in general become ubiquitous over the next decade...



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Pilot Lines



Current EU funded Pilot Lines




**ACT
PHAST**

Funded by:  
PHOTONICS PUBLIC PRIVATE PARTNERSHIP






LYTEUS
Flexible light

Funded by:  
PHOTONICS PUBLIC PRIVATE PARTNERSHIP





JePPIX
Pilot Line

Funded by:  
PHOTONICS PUBLIC PRIVATE PARTNERSHIP



Phabulous

Funded by:  
PHOTONICS PUBLIC PRIVATE PARTNERSHIP




MedPhab
Photonic Medical Devices

Funded by:  
PHOTONICS PUBLIC PRIVATE PARTNERSHIP






PIX4life

Funded by:  
PHOTONICS PUBLIC PRIVATE PARTNERSHIP





**Mid IR
Alliance**

Funded by:  
PHOTONICS PUBLIC PRIVATE PARTNERSHIP



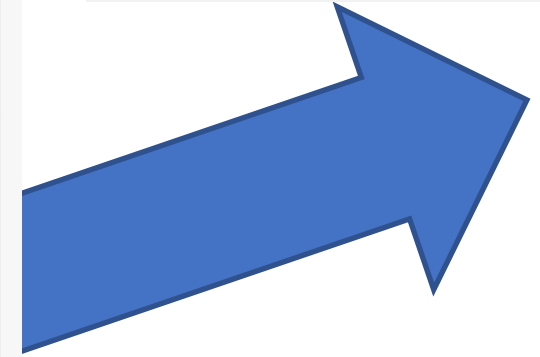
PIXAPP
Photonic Packaging
Pilot Line

Funded by:  
PHOTONICS PUBLIC PRIVATE PARTNERSHIP



**PhotonHub
Europe®**

Funded by:  
PHOTONICS PUBLIC PRIVATE PARTNERSHIP



Seeding a PIC infrastructure

PIC pilot lines

Pilot Line	Focus	Role	Status
Lyteus (PI Scale)	OLED lighting applications for displays, illumination, automotive	Provide prototyping runs before scale-up	Self-sustaining Open for opportunities
Mid IR Alliance (MIRPHAB)	Mid IR chemical sensor applications	Provide module designs in small volume	Self-sustaining Open for opportunities
PIX4LIFE	Dielectric PICs for bio-photonics and life science	Provide prototype PIC chips for scaling in volume	Self-sustaining Open for opportunities
PIXAPP	PIC packaging platforms for heavy data, medical, sensing	Provide PIC packaging and assembly services for PIC chips	Final year EU funding Open for opportunities
Jeppix (InPulse)	InP PIC foundry	Provide design, fabrication, test services to SMEs	Mid-course EU funding EU assistance on projects
Phabulous	Free-form micro-optics applications	Provide optical lenses for broad applications	Mid-course EU funding EU assistance on projects
MedPhab	Silicon photonics for medical, healthcare applications	Provide healthcare prototypes	Mid-course EU funding EU assistance on projects
Photon Hub	Building a photonics network infrastructure	To support SMEs/pilot line prototypes ramp prototypes	Mid-course EU funding to assist photonics SMEs
ACTPHAST	Creating an early-stage photonics infrastructure	To support SMEs/pilot line create prototypes	Mid-course EU funding to assist photonics academia & SMEs

Key metrics for all pilot lines

Industrial advisors (Review, advise, feedback)

- Monitor progress/focus on goals; Advise on issues/opportunities/markets



Strategic Issues (Making sure the plan succinct, credible, and fundable)

- Ready for business; Path to sustainability; Product offering, Financial and business model, competition, differentiation, Value proposition, KPIs (key performance indicators).



Demonstration cases (Customer interest → strong motivator)

- Synergies with products; Attracting new customers; Criteria for new applications/demo cases; Showing customers solutions for their business; Innovation for future offering.



Operational structure (Working towards single pilot line architecture)

- Seamless infrastructure with project members; Designing in flexibility; Evaluating maturity of platform technologies; Plans must show scalability, control, quality; Freedom of manufacturing



Open Access (Making it easy to use)

- Ensure openness, especially for SMEs, 'front office'



Publicity, marketing and communications (Market positioning → Reaching your customer)

- Reaching your customer-base; conveying credibility at technology/product shows/exhibits



Strong 'venture capital-like' metrics

Pilot line preparation for self-sustainability

~4yrs EU funding (it's seed funding)

- It's never too early to plan for self-sustainability. Plan for revenue generation in 3rd/4th year before funding expires; finalize legal agreements early (1st /2nd) year



The 1st products...

- What will they be? Like the demonstrators planned, or something different. Will they make money (or support the pilot line)? Have supporting customer interest...



Understand the customer and the market application

- Are you supplanting the customer's manufacturing line? Are you testing out new potential products for them in low volume? Who will get the volume business in the end? Is the market really ready?



Utilizing the support eco-system

- Leveraging PIC pilot lines, digital hubs, hybrid foundries, packaging and assembly houses



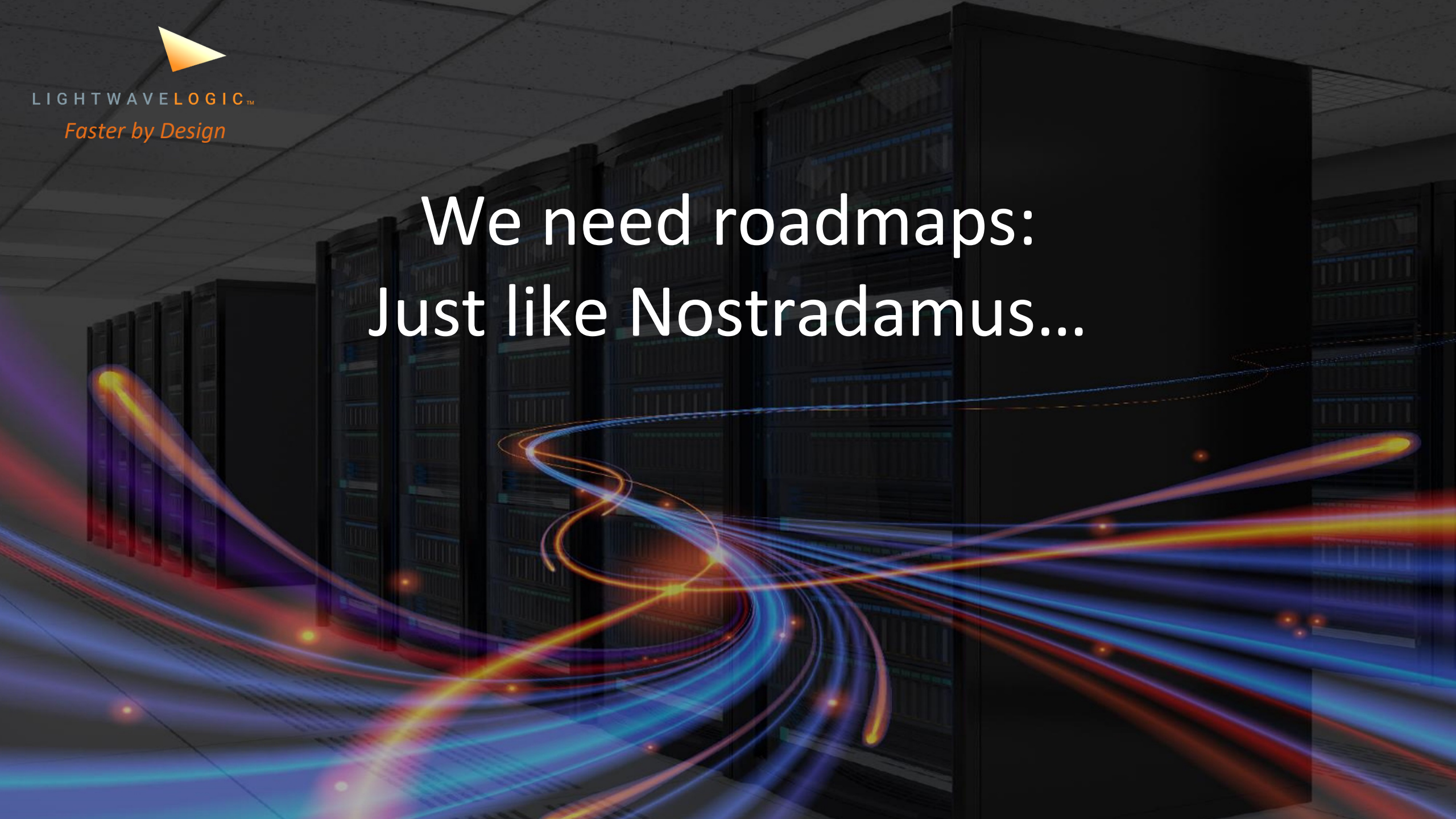
Positioning for self-sustainability → provide value in the manufacturing infrastructure

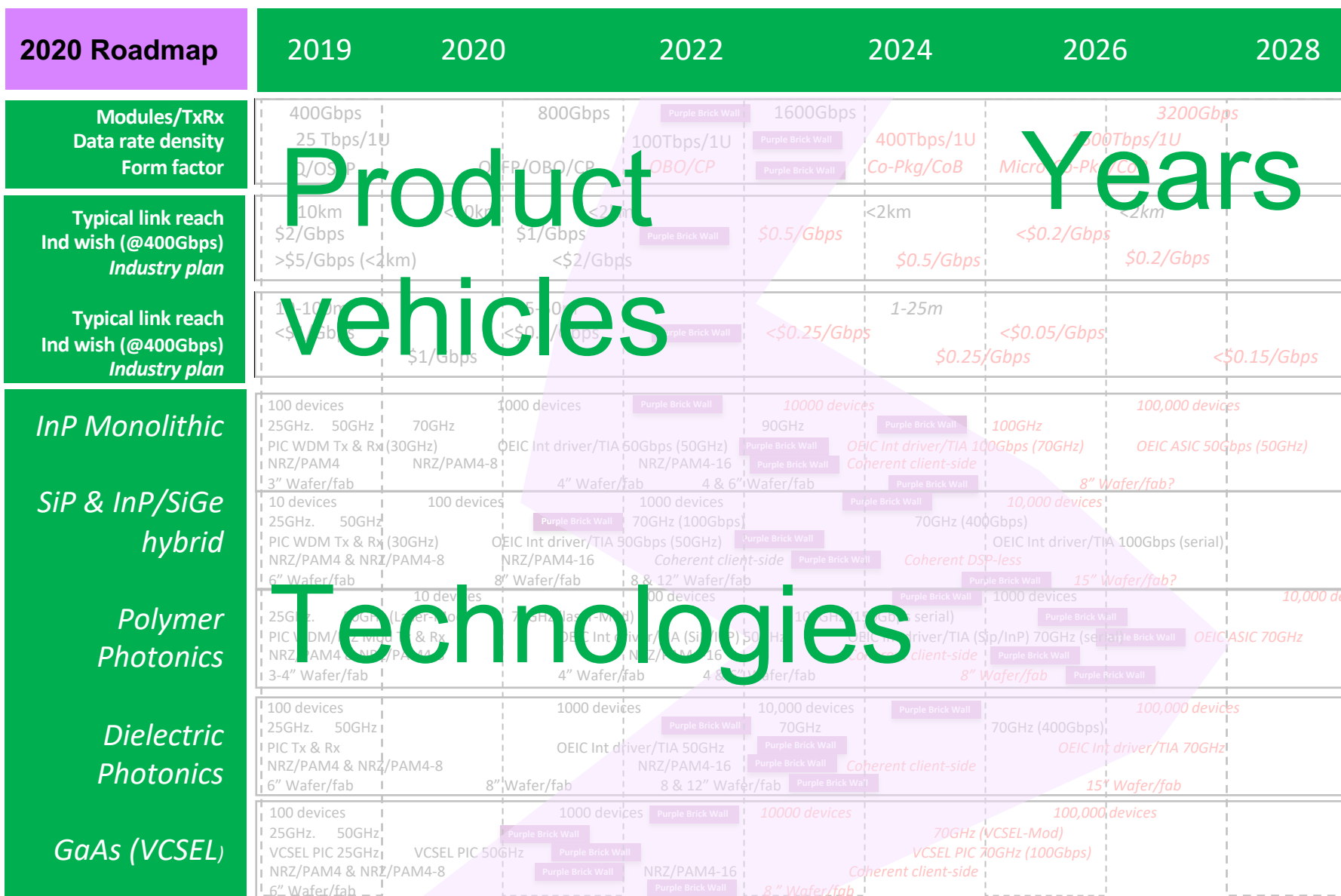


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We need roadmaps:
Just like Nostradamus...





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>1600Gbps+
TxRx
modules...

Tough to design
>70GHz
bandwidth
devices...

Some
technologies
have higher
performance....

How to
scale PIC
integration?

Product vehicles

Technologies

Normal Black Font = Reasonably expected based on current efforts
 Purple Brick Wall = Technology cost barrier
 Slanted Red Font = Major industry effort required for commercialization

Sources: LWLG, iNEMI, AIM Photonics, Photon Delta

2020 Roadmap	2019	2020	2022	2024	2026	2028
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Normal R&D funding

Major investment in R&D to achieve goals

Tough to design >1600Gbps+ TxRx modules...

Tough to design >70GHz bandwidth devices...

Some technologies have higher performance....

How to scale PIC integration?

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Red means major industry efforts needed for commercialization

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Purple brick wall = Technology cost barrier

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We may have photonics technology → but not at a cost for commercialization...

- Huge amount of data and small font...1-page...
- Details can be better viewed better *online*

Roadmaps provide a vehicle for all stakeholders: Gvt, industry, academia, bankers and investors...

2020 Roadmap	2019	2020	2022	2024	2026	2028
Modules/TxRx Data rate density Form factor	400Gbps 25 Tbps/1U Q/OSFP	800Gbps OSFP/OBO/CP	100Tbps/1U OBO/CP	1600Gbps 400Tbps/1U Co-Pkg/CoB	3200Gbps 1600Tbps/1U Micro-Co-Pkg/CoB	
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Where we penetrate the 'Purple Brick Wall'?

- A *1-page PIC packaging roadmap*...
- Details can be better viewed better *online*

Simple 1 slide roadmaps – have impact



2022 Roadmap (PIC Packaging)	2021	2022	2024	2026	2028	2030
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Traditional Gold Box	Butterfly 50GHz. Form factor: PIC chips <10 functions	100GHz micro-butterfly 10-50 functions	Purple Brick Wall	nano-butterfly 150GHz	200GHz	500 functions
Surface mount	SOIC (<50 lead) 25GHz. Connectorized SM/MM fiber Flip-chip bumping to pcb <100 bumps Thermal passive heat management	50GHz Fiber ribbons 1x12/24	micro-SOIC (<50 lead) 70GHz <250 bumps advanced thermal designs	70GHz (100Gbps NRZ) 2D fiber ribbons 2x24/48 <1000 bumps	100GHz (130Gbps NRZ) 2D fiber ribbons >500 fibers <10,000 bumps	
Chip-on-board & waferscale	Flip-chip bump (100) Interconnect bandwidth 25GHz. Wafer format 150mm Fiber to PIC packaging (grating/edge) 2D Integration	1000 devices 50GHz 200mm micro-optics to PIC packaging (grating/edge) 2.5D integration	10000 devices 70GHz	300mm 3D integration	100,000 devices 100GHz Interposer to PIC packaging (edge/evanescent)	200GHz 450mm
Co-packaging (layer 1 – chip on carrier)	2 chips 25GHz. 2D Integration (electronic IC on PIC) Active cooling (standard TEC) Passive cooling (std heat spreaders)	10 chips 50GHz 2.5D integration (electronic IC and PIC on carrier) Customized TEC/controller	30 chips 70GHz Graphene based materials	70GHz micro-TEC pkg with FIC Integrated with PIC Pkg.	50 chips 150GHz PIC on interposer (Optical) TEC integrated directly PIC Integrated with PIC	
Co-packaging (layer 2 -	10 devices 25GHz. Single die Optical platform 150mm Electronic and photonic PIC 2D package	50GHz twin die multiple die 2D Optical platform 200mm electronic and photonics PIC 2.5D package	100 devices 70GHz	multiple die 3D/fan out interconnect optical platform 300mm	1000 devices 150GHz multiple die 3D/double sided PIC 3D package platform	
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Source: Lightwave Logic, EPIC

A PIC Packaging roadmap...



As per the silicon electronics industry → Chip scale packaging (CSP-TAP)

2022 Roadmap (PIC Packaging)	2021	2022	2024	2026	2028	2030
Modules/TxRx Data rate density Form factor	400Gbps 25 Tbps/1U Q/OSFP	800Gbps OSFP/OBO/CP	100Tbps/1U OBO/CP	1600Gbps Co-Pkg/CoB	400Tbps/1U Micro-Co-Pkg/CoB	3200Gbps 1600Tbps/1U
Typical link reach Ind wish (@400Gbps) Industry plan	<10km \$2/Gbps >\$5/Gbps (<2km)	<10km \$1/Gbps <\$2/Gbps	<2km Purple Brick Wall	<2km \$0.5/Gbps Purple Brick Wall	<2km \$0.5/Gbps	<2km \$0.2/Gbps
Typical link reach Ind wish (@400Gbps) Industry plan	10-100m <\$1/Gbps	5-50m <\$0.5/Gbps	5-50m Purple Brick Wall	1-25m <\$0.25/Gbps Purple Brick Wall	1-25m \$0.25/Gbps	<\$0.15/Gbps
Traditional Gold Box	Butterfly 50GHz. Form factor: PIC chips <10 functions	100GHz micro-butterfly 10-50 functions	150GHz nano-butterfly 100-200 functions	200GHz Purple Brick Wall	500 functions	
Surface mount	SOIC (<50 lead) 25GHz. Connectorized SM/MM fiber Flip-chip bumping to pcb <100 bumps Thermal passive heat management	50GHz micro-SOIC (<50 lead) Fiber ribbons 1x12/24	70GHz (100Gbps NRZ) <250 bumps advanced thermal designs	100GHz (130Gbps NRZ) 2D fiber ribbons 2x24/48 <1000 bumps	100GHz (130Gbps NRZ) 2D fiber ribbons <10,000 bumps	
Chip-on-board & waferscale	Flip-chip bump (100) Interconnect bandwidth 25GHz. Wafer format 150mm Fiber to PIC packaging (grating/edge) 2D Integration	1000 devices 50GHz 200mm micro-optics to PIC packaging (grating/edge) 2.5D integration	10000 devices 70GHz 300mm 3D integration	100,000 devices 100GHz Interposer to PIC packaging (edge/evanescent)	200GHz	
Co-packaging (layer 1 – chip on carrier)	2 chips 25GHz. 2D Integration (electronic IC on PIC) Active cooling (standard TEC) Passive cooling (std heat spreaders)	10 chips 50GHz 2.5D integration (electronic IC and PIC on carrier) Customized TEC/controller	30 chips 70GHz Purple Brick Wall Graphene based materials.	50 chips 150GHz Purple Brick Wall micro-TEC pkg with PIC Integrated with PIC Pkg.	50 chips 150GHz Purple Brick Wall PIC on interposer (Optical) TEC integrated directly PIC Integrated with PIC	
Co-packaging (layer 2 -	10 devices 25GHz. Single die Optical platform 150mm Electronic and photonic PIC 2D package	50GHz twin die Optical platform 200mm electronic and photonics PIC 2.5D package	100 devices 70GHz multiple die 2D Optical platform 200mm	1000 devices 150GHz multiple die 3D/fan out interconnect optical platform 300mm	1000 devices 150GHz multiple die 3D/double sided PIC 3D package platform	
	Normal Black Font = Reasonably expected based on current efforts		Purple Brick Wall = Technology cost barrier		Slanted Red Font = Major industry effort required for commercialization	

Source: Lightwave Logic, EPIC

A PIC Packaging roadmap...trends towards chip scale packaging/Testing-Assembly-Packaging (CSP-TAP)



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Creating a PIC infrastructure

→ Competitive positioning

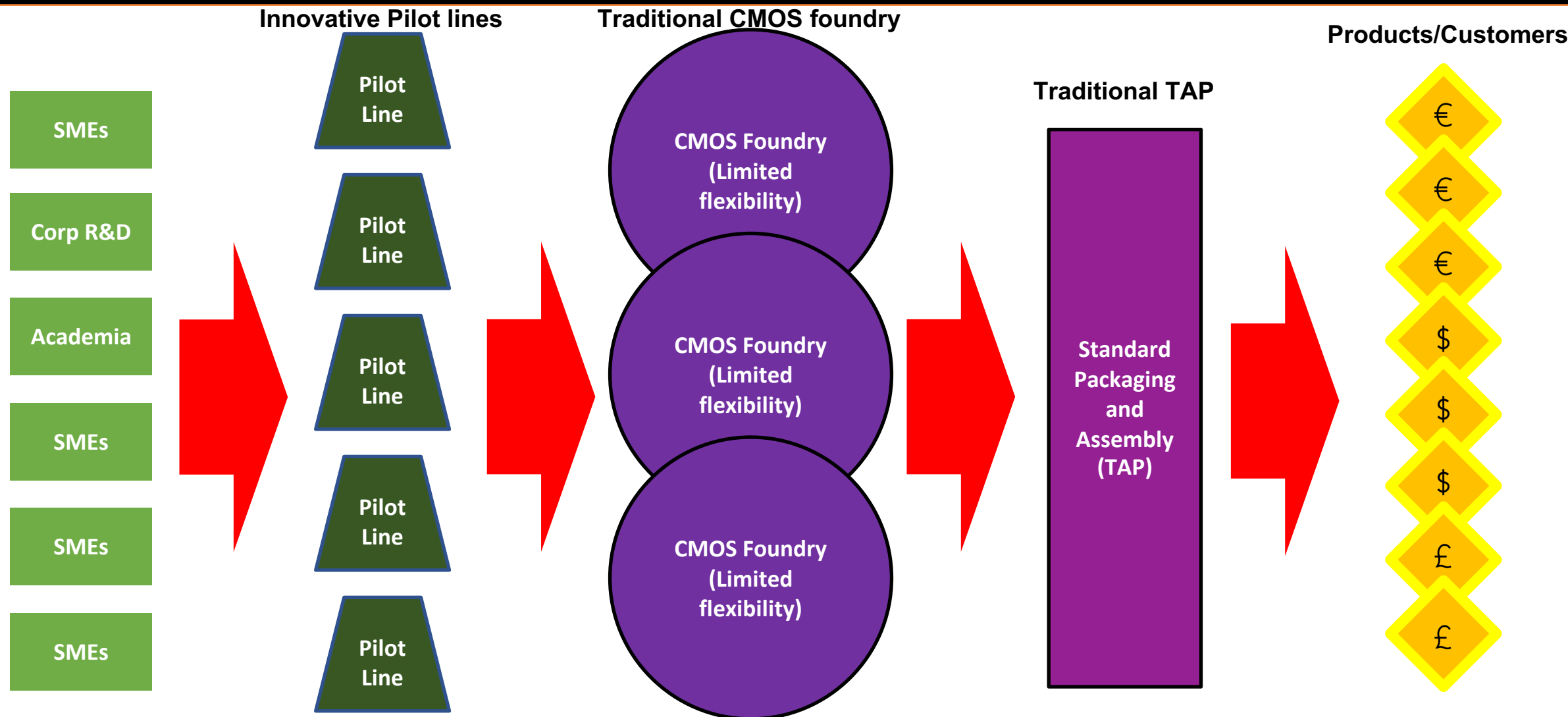
How to win?

Report Card

- Provide easier access for SMEs...*they drive innovation...* ✓
- Create more PIC pilot line scale projects...*that impact growing markets* ✓
 - Auto, medical, sensing, display etc.
- Create a sharper focus...*foundries for PICs* ?
- Create PIC packaging centers...*for chip-scale packaging* ?
- Utilize the framework of digital hubs... *e.g. PhotonHUB* ✓

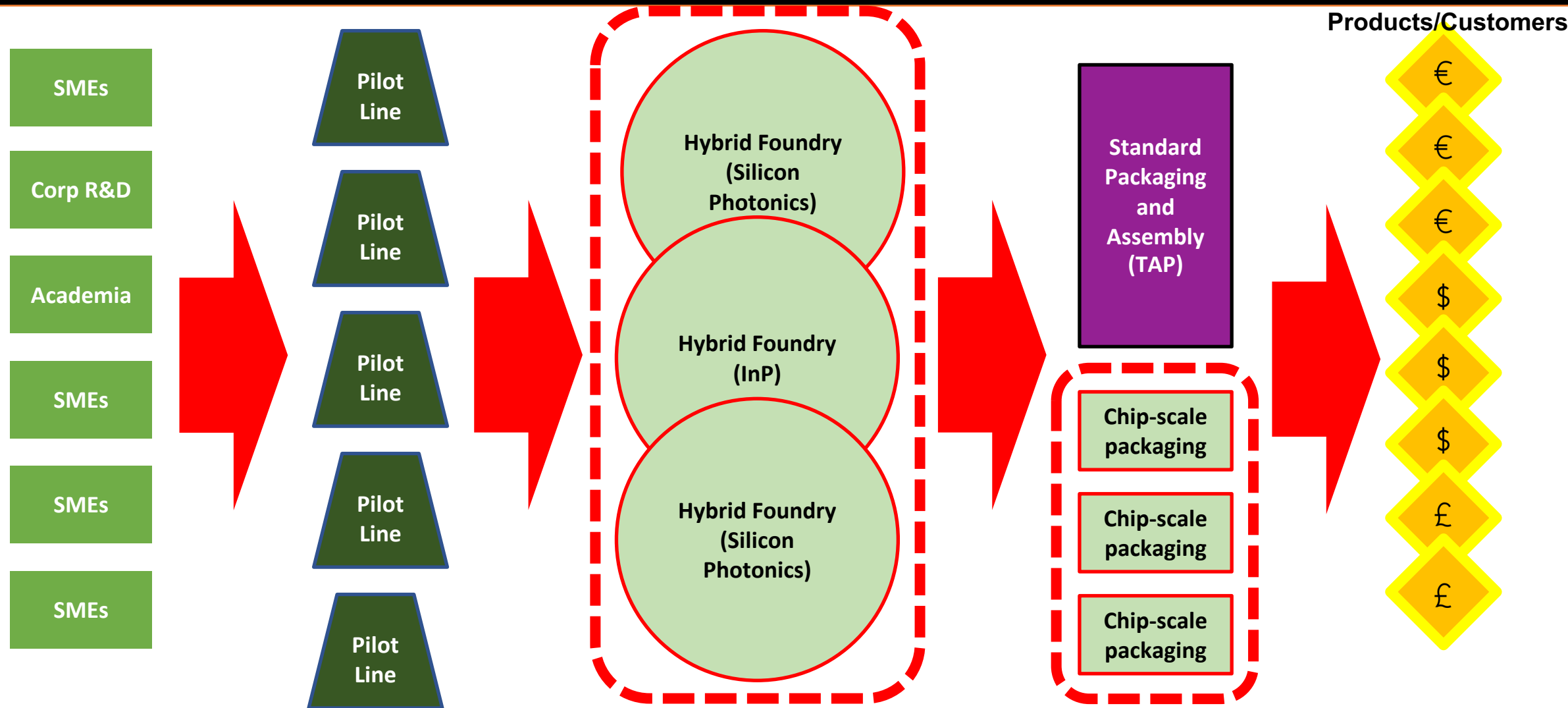
Build into a global center of excellence...

Simplified route for PICs today...



Limited flexibility with foundry and packaging/TAP

“Weaknesses” in PIC ‘Hub-Spoke’ architecture



More flexibility is needed for PICs to harness more performance

- Hybrid PIC

- It is not a pure play PIC (i.e. not pure InP or pure silicon photonics)
- It is a mix and match of dissimilar technologies to **improve overall performance**
- Examples are lasers, SiGe, electro-optic polymers, dielectrics, glass, Barium Titanate, Lithium Niobate, Plasmonics etc.

- Hybrid Foundry

- A foundries that can run the base PIC platform (e.g. silicon photonics, InP, GaAs) and is **flexible to run other dissimilar technologies** that improve overall performance.
- The trade-off is between standard CMOS PDKs and innovative PICs that require novel PDKs

- Chip-Scale-Packaging/TAP (CSP-TAP)

- Follow the electronics route and discard the package – mount the chips directly to the sub-mount/pcb; use optics in the pcb...

Adding Hybrid foundry and CSP/TAP center to strengthen the infrastructure...



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Summary



3 questions to remember today...

- Can the PIC pilot lines provide product value?
 - **YES...and we need more of them...**
- Can we integrate the PIC pilot lines into a competitive infrastructure environment?
 - **We can but the PIC infrastructure is not quite complete...**
- What's needed to make sure our PIC infrastructure is successful in manufacturing over the next decade?
 - **At least 1 hybrid foundry...more PIC pilot lines**
 - **Chip-scale-packaging/TAP house for PICs...**

} € 300-500M

Creates a competitive, innovative, flexible EU PIC infrastructure...and highly differentiated...



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END





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Back-up

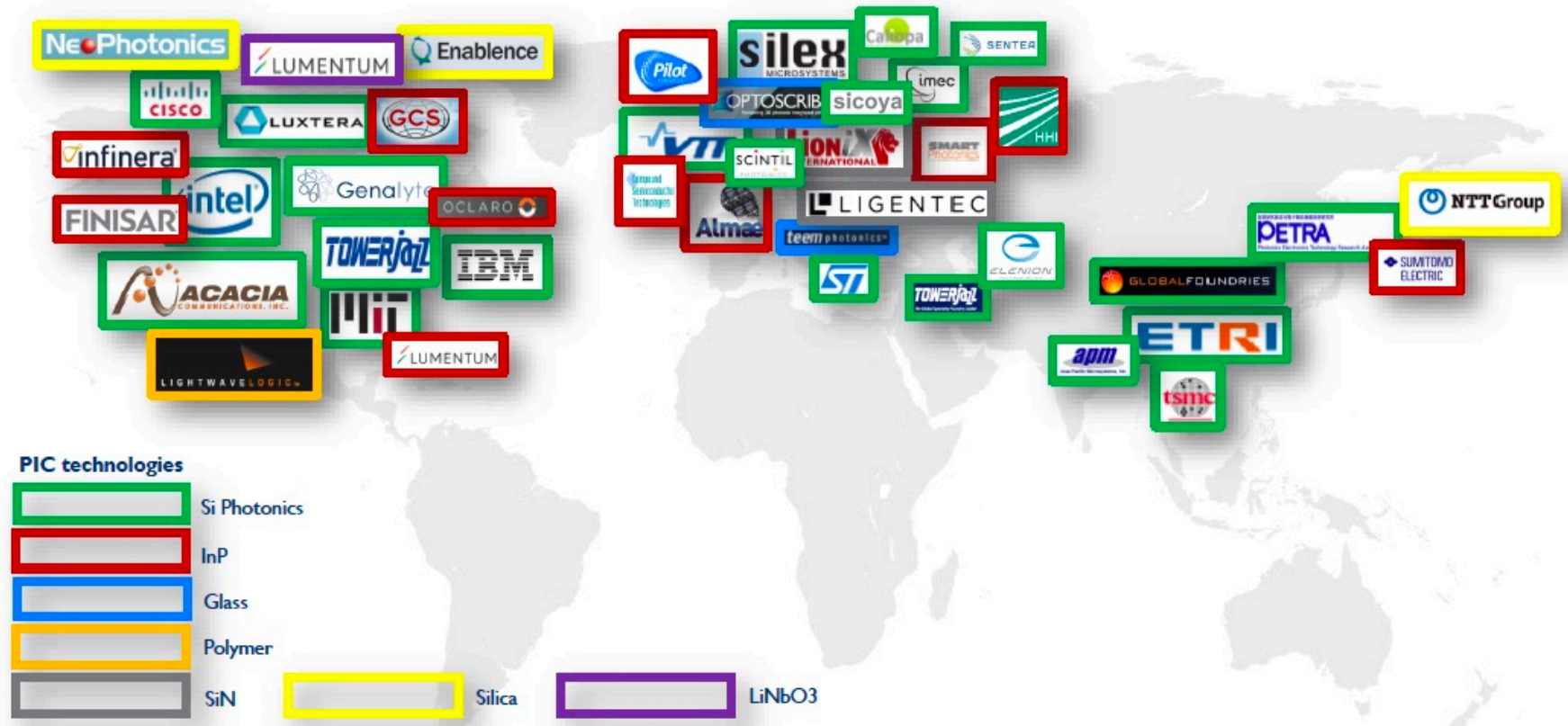


- Historic incumbent:
 - InP (Indium Phosphide)
 - GaAs (Gallium Arsenide)
- New incumbent:
 - SiP (Silicon photonics)
- ***New platforms and hybrid accelerators for PICs***
 - *Polymer, dielectrics, glass, lithium niobate thin film, plasmonic, barium titanate, silica, germanium etc.*

Silicon photonics is the new kid on the block; new platforms → hybrid PICs

Sample global players and their PIC platforms

- Growth of Silicon photonics
- Trend towards hybrid platforms for PICs
- What combinations of technology make sense for hybrid PICs?



Challenge is to further PIC performance with other materials → hybrid PICs

Industry has 2 incumbent PICs...

Incumbent

Incumbent

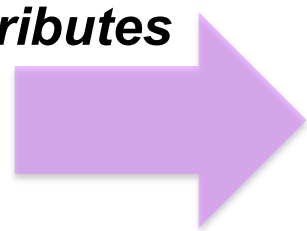
Indium Phosphide

Silicon Photonics

All InP

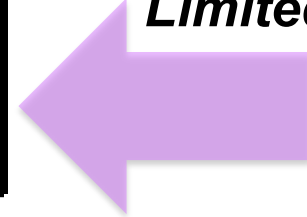
All SiPh

Limited attributes



- InP laser ✓
- InP passives ✓
- InP modulator ✓ (limited)
- InP electronics ✓ (limited)

Limited attributes



- Si laser ☒
- SiPh passives ✓
- Si modulator (limited)
- Si electronics ✓

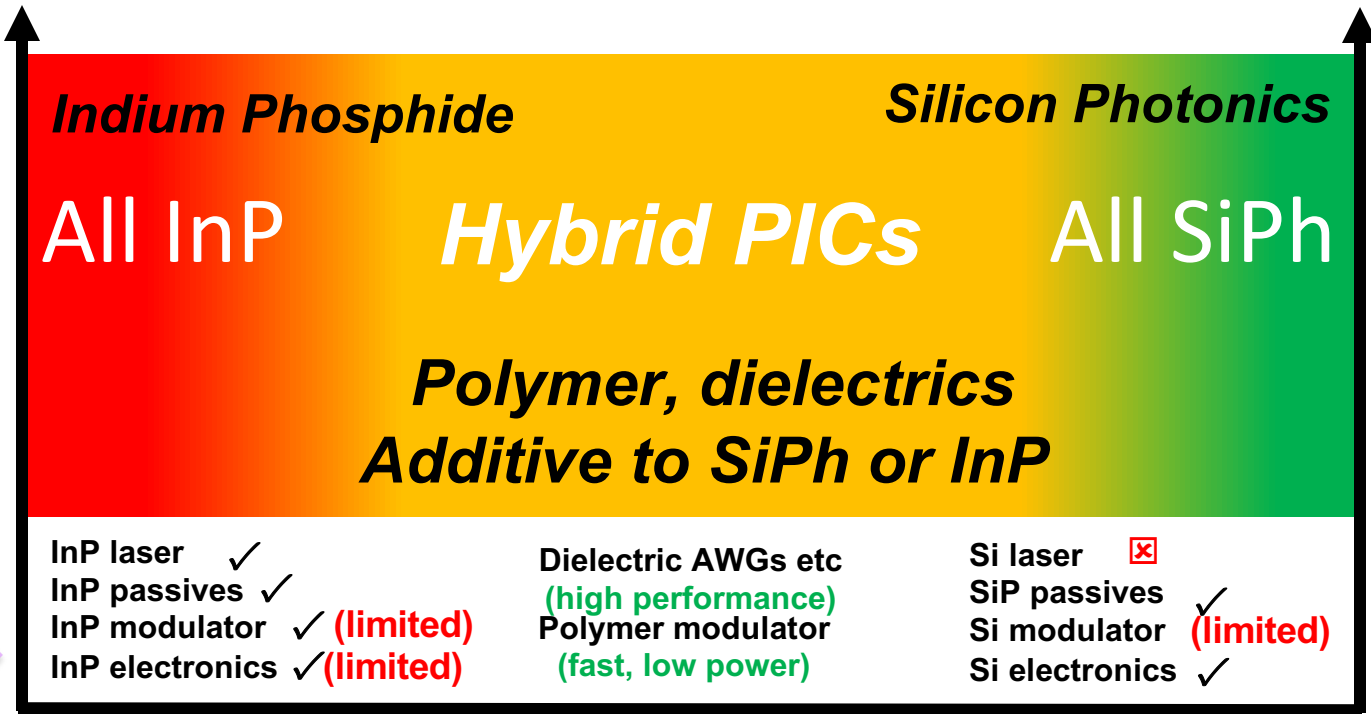
Incumbent technologies can't do everything...need help from hybrid PIC technologies...

Hybrid PICs increase performance...

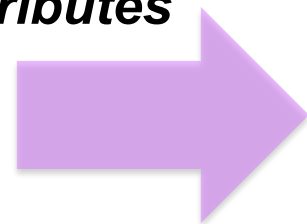
New hybrid PICs

Incumbent

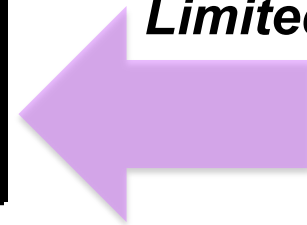
Incumbent



Limited attributes



Limited attributes



Hybrid PICs can boost performance of PICs