



LIGHTWAVE LOGIC

Faster by Design

Hybrid photonic integration roadmap

Michael Lebbby, CEO
Lightwave Logic (NASDAQ:LWLG)

A server room with rows of black server racks. The scene is illuminated by vibrant, glowing light trails in shades of blue, orange, and purple that swirl and flow through the space, creating a sense of dynamic energy and data movement. The text 'Hybrid PIC...' is centered in the foreground in a white, bold, sans-serif font.

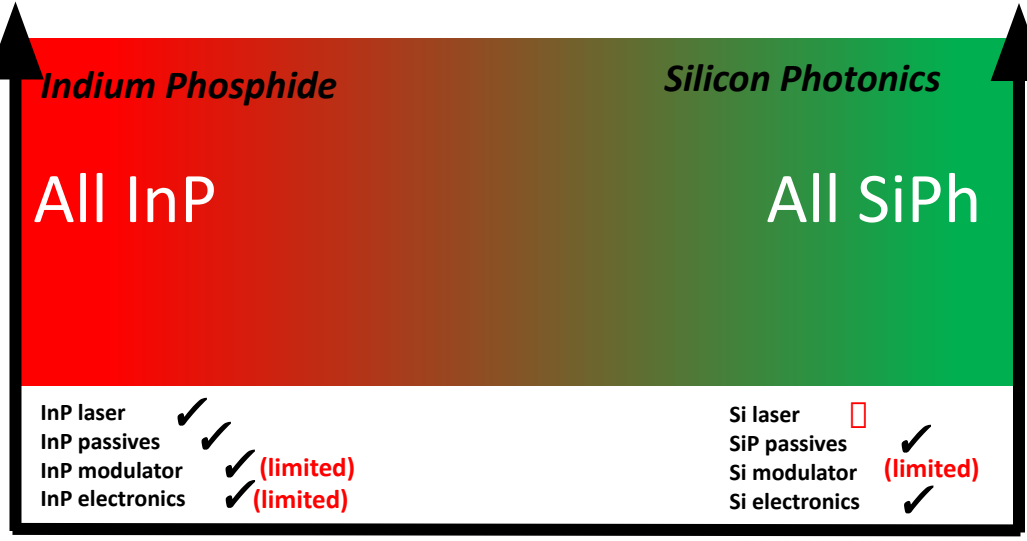
Hybrid PIC...

Fiber communications have 2 incumbent PICs, however...



LIGHTWAVE

Incumbent *Incumbent*



Limited attributes



Limited attributes



Incumbent technologies can't do everything monolithically...

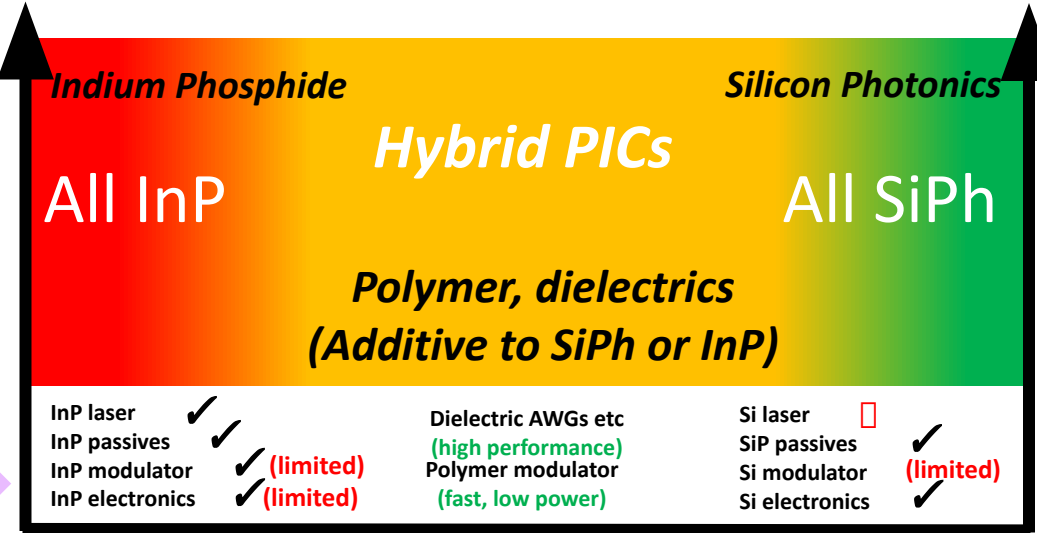


Hybrid PICs increase performance...

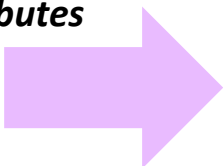
New hybrid PICs

Incumbent

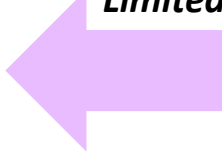
Incumbent



Limited attributes



Limited attributes



Hybrid solutions

Hybrid PICs can boost performance of PICs



Trend towards hybrid PICs...

- PIC incumbent platforms:
 - InP (Indium Phosphide) □ e.g. Hybrid PIC □ InP + Si ICs
 - SiPh (Silicon photonics) □ e.g. Hybrid PIC □ SiPh + InP Laser

• ***New platforms for Hybrid PICs***

- *Polymers (modulators)*
- *Dielectrics (passives)*
- *Silica (passives)*
- *Glass (passives)*
- *Thin Film Lithium Niobate (TFLN) (modulators)*
- *Metal/plasmonic, (modulators)*
- *Barium titanate (BTO) (modulators)*
- *Germanium (detectors)*
- *Gallium Nitride (GaN) (LEDs)*
- ***Many others...***

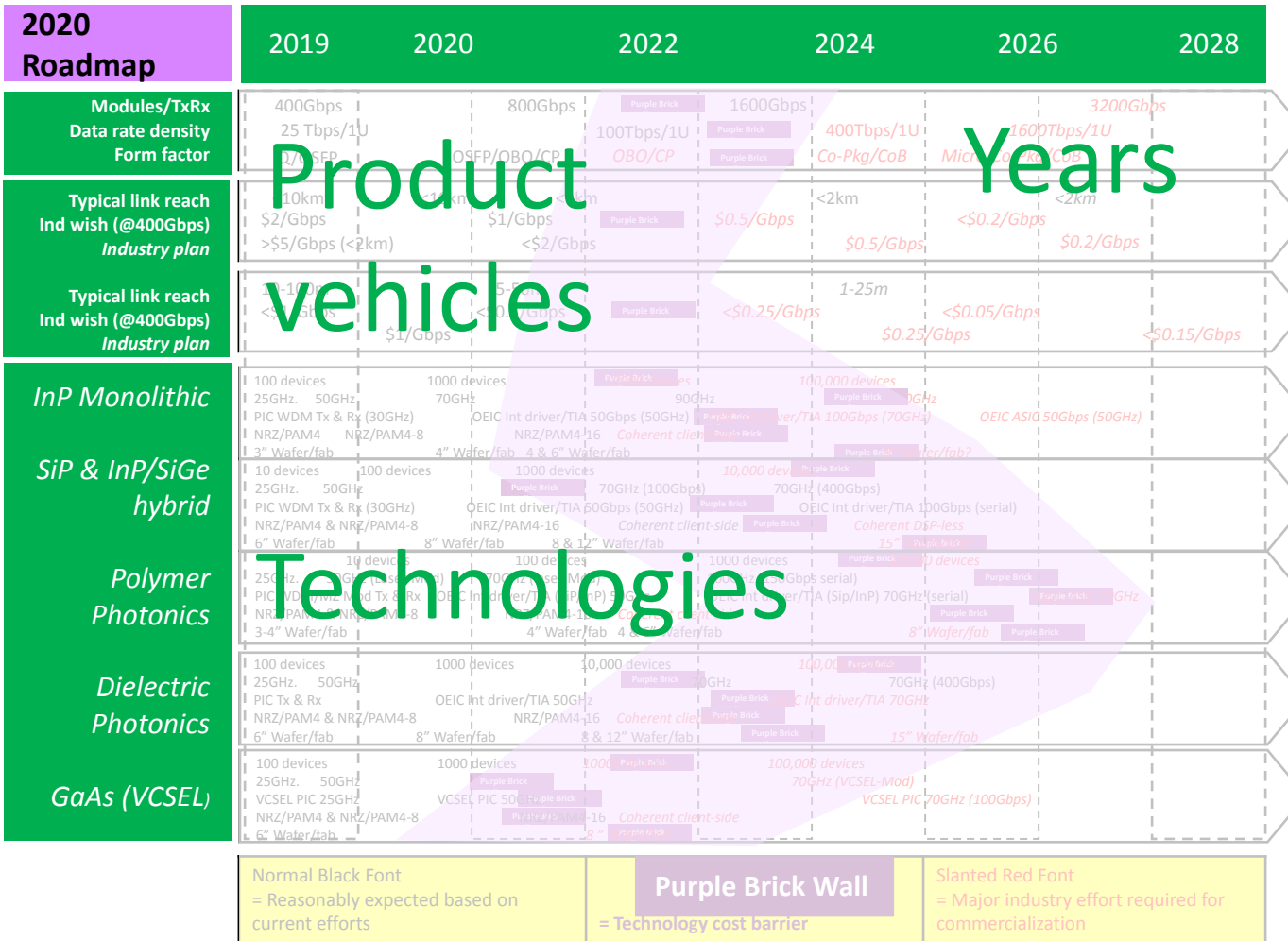
Mix and match to optimize the best performance...

A server room with rows of black server racks. The scene is illuminated by vibrant, glowing light trails in shades of blue and orange, creating a sense of motion and data flow. The text is overlaid in the center of the image.

**We need roadmaps:
Just like Nostradamus....**

A server room with rows of black server racks. The scene is illuminated with vibrant, glowing light trails in shades of blue, orange, and purple, creating a sense of motion and data flow. The text "Roadmap 2020" is prominently displayed in the center in a white, bold, sans-serif font.

Roadmap 2020



Tough to design
>1600Gbps+
TxRx
modules...

Tough to design
>70GHz
bandwidth
devices...

Some
technologies have
higher
performance....

How to scale
PIC
integration?

Simple metrics

2020 Roadmap	2019	2020	2022	2024	2026	2028
Modules/TxRx Data rate density Form factor	400Gbps 25 Tbps/1U Q/OSFP	800Gbps OSFP/OBO/CP	1600Gbps 100Tbps/1U OBO/CP	3200Gbps 400Tbps/1U Co-Pkg/CoB	6400Gbps 1600Tbps/1U Micro-Co-Pkg/CoB	12800Gbps 3200Gbps
Typical link reach Ind wish (@400Gbps) Industry plan	<10km \$2/Gbps >\$5/Gbps (<2km)	<10km \$1/Gbps	<2km \$0.5/Gbps	<2km \$0.2/Gbps	<2km \$0.2/Gbps	<2km \$0.2/Gbps
Typical link reach Ind wish (@400Gbps) Industry plan	10-100m <\$1/Gbps	5-50m \$1/Gbps <\$0.5/Gbps	1-25m \$0.25/Gbps	1-25m \$0.25/Gbps	1-25m \$0.05/Gbps	1-25m \$0.15/Gbps
InP Monolithic	100 devices 25GHz 50GHz PIC WDM Tx & Rx (30GHz)	1000 devices 70GHz OEIC Int driver/TIA (SiP/InP) 50GHz	1000 devices 90GHz OEIC Int driver/TIA (SiP/InP) 50GHz	1000 devices 100GHz (15 Gbps serial) OEIC Int driver/TIA (SiP/InP) 70GHz	1000 devices 100GHz (15 Gbps serial) OEIC Int driver/TIA (SiP/InP) 70GHz	1000 devices 100GHz (15 Gbps serial) OEIC Int driver/TIA (SiP/InP) 70GHz
SiP & InP/SiGe hybrid	10 devices 25GHz 50GHz PIC WDM/MZ Mpd Tx & Rx	100 devices 70GHz (laser-M4d) OEIC Int driver/TIA (SiP/InP) 50GHz	1000 devices 100GHz (15 Gbps serial) OEIC Int driver/TIA (SiP/InP) 70GHz	1000 devices 100GHz (15 Gbps serial) OEIC Int driver/TIA (SiP/InP) 70GHz	1000 devices 100GHz (15 Gbps serial) OEIC Int driver/TIA (SiP/InP) 70GHz	1000 devices 100GHz (15 Gbps serial) OEIC Int driver/TIA (SiP/InP) 70GHz
Polymer Photonics	NRZ/PAM4 & NRZ/PAM4-8 3-4" Wafer/fab	NRZ/PAM4-16 4" Wafer/fab	NRZ/PAM4-16 4" Wafer/fab	NRZ/PAM4-16 4" Wafer/fab	NRZ/PAM4-16 4" Wafer/fab	NRZ/PAM4-16 4" Wafer/fab
Dielectric Photonics	NRZ/PAM4 & NRZ/PAM4-8 6" Wafer/fab	NRZ/PAM4-16 8" Wafer/fab	NRZ/PAM4-16 8 & 12" Wafer/fab	NRZ/PAM4-16 8 & 12" Wafer/fab	NRZ/PAM4-16 8 & 12" Wafer/fab	NRZ/PAM4-16 8 & 12" Wafer/fab
GaAs (VCSEL)	100 devices 25GHz 50GHz VCSEL PIC 25GHz	1000 devices VCSEL PIC 50GHz	1000 devices VCSEL PIC 50GHz	1000 devices VCSEL PIC 50GHz	1000 devices VCSEL PIC 50GHz	1000 devices VCSEL PIC 50GHz

Normal R&D funding

Major investment in R&D to achieve goals

- Tough to design >1600Gbps+ TxRx modules...
- Tough to design >70GHz bandwidth devices...
- Some technologies have higher performance....
- How to scale PIC integration?

Normal Black Font = Reasonably expected based on current efforts
 Purple Brick Wall = Technology cost barrier
 Slanted Red Font = Major industry effort required for commercialization

Red means major industry efforts needed for commercialization

2020 Roadmap	2019	2020	2022	2024	2026	2028
Modules/TxRx	400Gbps	800Gbps	1600Gbps	3200Gbps	6400Gbps	12800Gbps
Data rate density	25 Tbps/1U	50 Tbps/1U	100 Tbps/1U	200 Tbps/1U	400 Tbps/1U	800 Tbps/1U
Form factor	Q/OSFP	OSFP/OBO/CP	OBO/CP	Co-Pkg/CoB	Micro-Co-Pkg/CoB	
Typical link reach	<10km	<10km	<2km	<2km	<2km	<2km
Ind wish (@400Gbps)	\$2/Gbps	\$1/Gbps	\$0.5/Gbps	\$0.25/Gbps	\$0.15/Gbps	\$0.1/Gbps
Industry plan	>\$5/Gbps (<2km)	\$1/Gbps	<\$0.5/Gbps	<\$0.25/Gbps	<\$0.15/Gbps	<\$0.1/Gbps
Typical link reach	10-100m	5-50m	1-25m	1-25m	1-25m	1-25m
Ind wish (@400Gbps)	<\$1/Gbps	\$1/Gbps	<\$0.5/Gbps	<\$0.25/Gbps	<\$0.15/Gbps	<\$0.1/Gbps
Industry plan		\$1/Gbps	<\$0.5/Gbps	<\$0.25/Gbps	<\$0.15/Gbps	<\$0.1/Gbps
InP Monolithic	100 devices	1000 devices	10,000 devices	100,000 devices	1,000,000 devices	10,000,000 devices
SiP & InP/SiGe hybrid	10 devices	100 devices	1000 devices	10,000 devices	100,000 devices	1,000,000 devices
Polymer Photonics	10 devices	100 devices	1000 devices	10,000 devices	100,000 devices	1,000,000 devices
Dielectric Photonics	100 devices	1000 devices	10,000 devices	100,000 devices	1,000,000 devices	10,000,000 devices
GaAs (VCSEL)	100 devices	1000 devices	10,000 devices	100,000 devices	1,000,000 devices	10,000,000 devices

Purple brick wall = Technology cost barrier

- Tough to design >1600Gbps+ TxRx modules...
- Tough to design >70GHz bandwidth devices...
- Some technologies have higher performance....
- How to scale PIC integration?

Normal Black Font = Reasonably expected based on current efforts

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We may have photonics technology but not at a cost for commercialization...



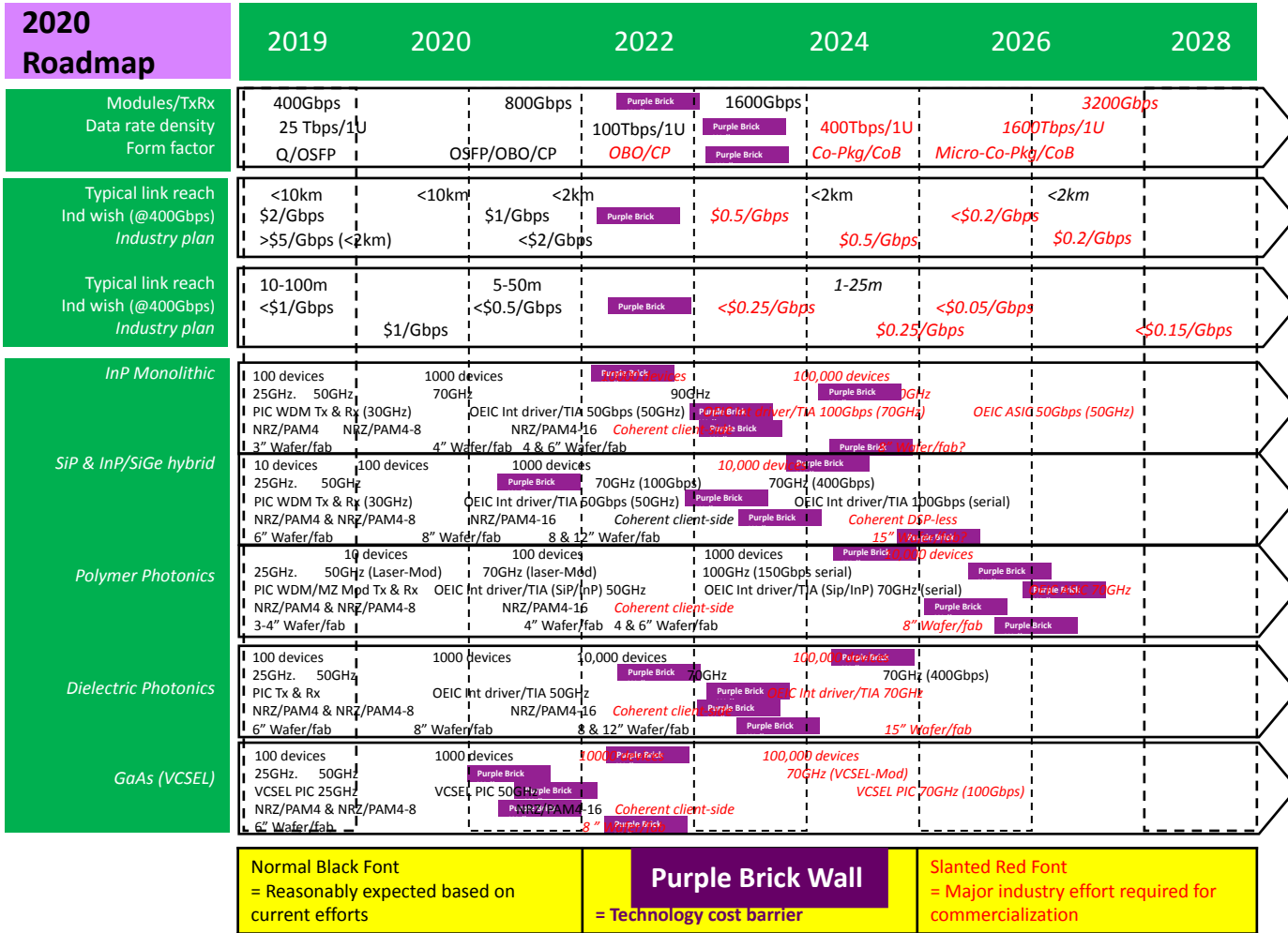
Roadmap 2020 (OLD)

Warning - Eye-chart!

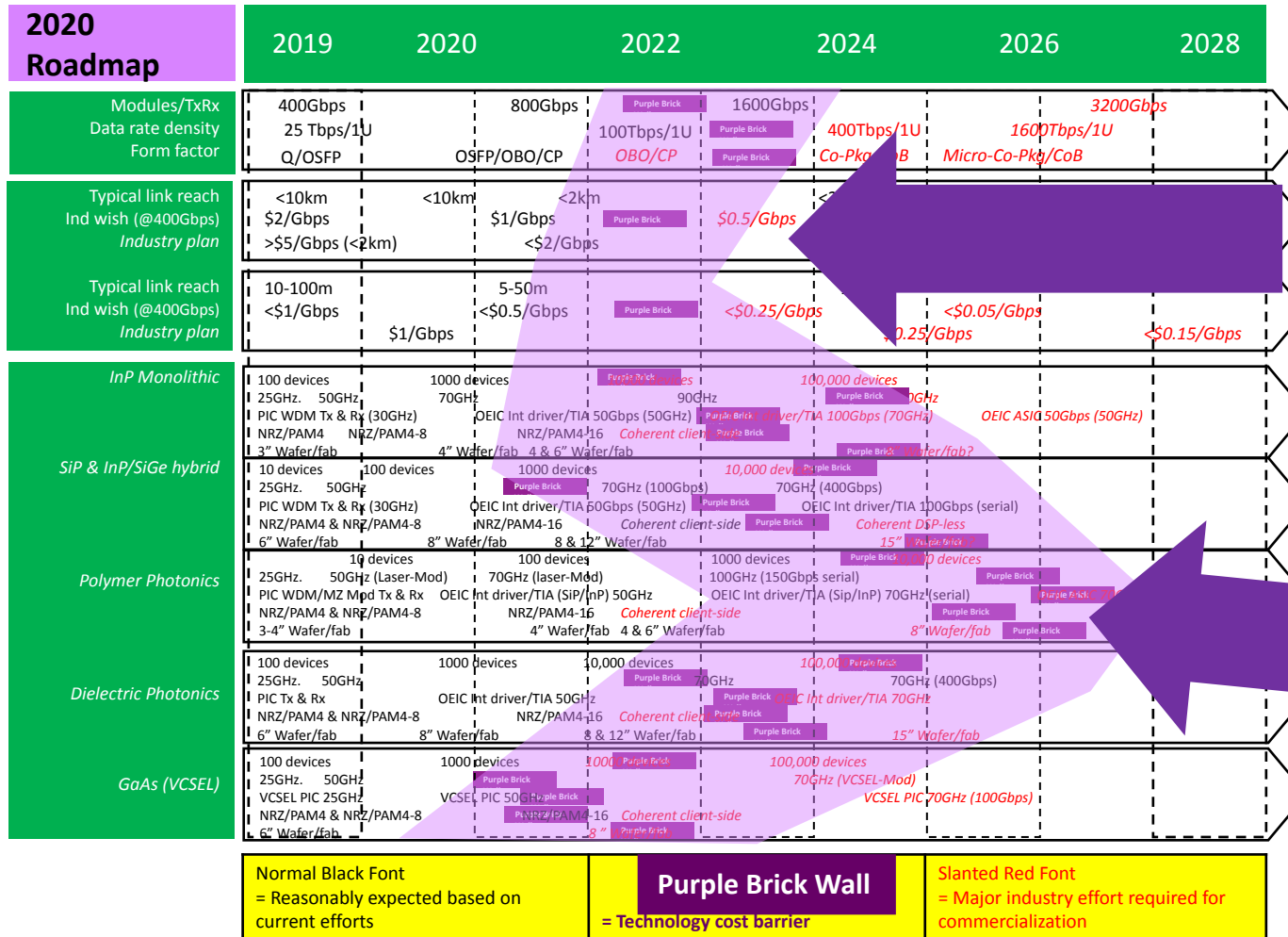
Don't try and read it – zoom soon
(can be found at www.lightwavelogic.com)



2020 PIC roadmap (datacom)



Years vs product vehicles vs technologies



Tough to design >1600Gbps TxRx modules...

Tough to design >70GHz bandwidth devices...

Some technologies have higher performance....

Normal Black Font = Reasonably expected based on current efforts

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Where we penetrate the 'Purple Brick Wall'?

A server room with rows of black server racks. The scene is illuminated with vibrant, glowing light trails in shades of blue and orange, creating a sense of motion and digital energy. The text is overlaid in the center of the image.

New!
Draft roadmaps 2022



Hybrid PIC roadmap - datacom

2022 Roadmap	2022	2024	2026	2028	2030.....2040	
Modules/TxRx Data rate density Form factor	800Gbps 25 Tbps/1U Q/OSFP	1600Gbps 50Tbps/1U OSFP/OBO/CP	3200Gbps 100Tbps/1U OSFP/OBO/CP	6.4Tbps 400Tbps/1U Micro-OSFP/OBO/CP	12.8Tbps 800Tbps/1U	25.2Tbps 50.4Tbps
Typical link reach Ind wish (@800Gbps) Industry plan	<10km <\$1/Gbps	<10km \$0.5/Gbps	<2km \$0.25/Gbps	<2km \$0.1/Gbps	<2km \$0.05/Gbps	<2km \$0.025/Gbps
Typical link reach Ind wish (@800Gbps) Industry plan	10-100m <\$0.5/Gbps	5-100m \$0.25/Gbps	5-100m \$0.1/Gbps	1-100m \$0.05/Gbps	1-100m \$0.025/Gbps	1-100m \$0.0125/Gbps
ACTIVE PLATFORM						
<i>Silicon Photonics</i>	TW carrier inj	TW carrier inj	Micro Ring resonator	Micro Ring resonator		
<i>Modulator</i>	25-35GHz (4-6V)	35GHz (3-6V)	50GHz (2-6V)	70GHz (2-6V)		
<i>Indium Phosphide</i>	PIC DD/Coherent	DFB/DBR/SOA	1310/1550nm	OEIC Tx/Rx DD/Coh with MSI	OEIC Tx/Rx DD/Coh with LSI	
<i>Laser/Modulator</i>	30-40GHz (1-4V)	35-50GHz (1-5V)	50GHz (2-8V)	80GHz (3-10V)		
<i>EO Polymer</i>	Slot waveguide	1310/1550nm	Integrated PIC slot W/G	1310/1550nm		
<i>Modulator</i>	70GHz (<1V)	100GHz (<0.5V)	110GHz (<0.5)	150GHz (<1V)	170GHz	
<i>Metal/plasmonic EO polymer</i>	Slot L/E PIC	1310/1550nm	Coh/DD slot L/E PIC	1310/1550nm		
<i>Modulator</i>	100GHz (5-10V)	150GHz (3-8V)	200GHz (1-5V)	300GHz (1-3V)	400GHz	
<i>BTO</i>	Integrated with SiPh/CMOS	Integrated PIC with CMOS				
<i>Modulator</i>	20-30GHz	30-40GHz	50GHz	70GHz		
<i>TFLN</i>	Multi-channel array	Integrated PIC with SiPh	Integrated PIC with CMOS			
<i>Modulator</i>	50GHz (3-8V)	70GHz (2-5V)	90GHz (2-5V)	100GHz		
PASSIVE PLATFORM						
<i>Silicon Photonics</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source	50GHz	SSI OEIC IC+SiPh w/LD/MRR	MSI OEIC IC+SiPh + LD/MRR		
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	80GHz		
<i>Dielectric/Glass/Silica</i>	PIC w/Mux/SSC/PD/GC + LD source		SSI PIC with SiPh w/LD/Hybrid modulator	MSI PIC with SiPh w/LD/Hybrid modulator		
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	100GHz	120GHz	
<i>InP</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source		SSI OEIC w/Hybrid modulator	MSI OEIC w/Hybrid modulator		
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	100GHz	120GHz	
<i>Polymer</i>	Integrated PCB/Interposer w/Mux/SSC/PD/GC + LD source		PCB/Interposer w/Mux/SSC/PD/GC w/LD/Hybrid modulator			
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	80GHz	90GHz	

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Hybrid PIC roadmap - datacom

2022 Roadmap	2022	2024	2026	2028	2030.....2040	
Modules/TxRx Data rate density Form factor	800Gbps 25 Tbps/1U Q/OSFP		600Gbps 100Tbps/1U O/CP	Purple Brick Wall 100Tbps/1U OSFP/OBO/CP	3200Gbps 6.4Tbps Purple Brick Wall	12.8Tbps 25.2Tbps 800Tbps/1U Micro-OSFP/OBO/CP	50.4Tbps
Typical link reach Ind wish (@800Gbps) Industry plan	<10km <\$1/Gbps	<10km \$0.5/Gbps	<2km <\$1/Gbps	Purple Brick Wall \$0.25/Gbps	<2km <\$0.5/Gbps	<2km <\$0.1/Gbps	<2km <\$0.1/Gbps
Typical link reach Ind wish (@800Gbps) Industry plan	10-100m <\$0.5/Gbps \$1-3/Gbps	5-100m <\$0.5/Gbps	5-100m <\$0.5/Gbps	Purple Brick Wall <\$0.1/Gbps	1-100m \$0.25/Gbps	1-100m <\$0.05/Gbps <\$0.15/Gbps	
ACTIVE PLATFORM							
<i>Silicon Photonics</i>	TW carrier inj	TW carrier inj	Micro Ring resonator	Micro Ring resonator			
<i>Modulator</i>	25-35GHz (4-6V)	35GHz (3-6V)	50GHz (2-6V)	70GHz (2-6V)			
<i>Indium Phosphide</i>	PIC DD/Coherent DFB/DBR/SOA	1310/1550nm	OEIC Tx/Rx DD/Coh with MSI	OEIC Tx/Rx DD/Coh with LSI			
<i>Laser/Modulator</i>	30-40GHz (1-4V)	35-50GHz (1-4V)					
<i>EO Polymer</i>	Slot waveguide	1310/1550nm	Integrated PIC slot W/G	1310/1550nm			
<i>Modulator</i>	70GHz (<1V)	100GHz (<0.5V)	110GHz (<0.5V)	150GHz (<1V)	170GHz		
<i>Metal/plasmonic EO polymer</i>	Slot L/E PIC	1310/1550nm	150GHz (3-8V)	200GHz (2-5V)	300GHz (2-5V)	400GHz	
<i>Modulator</i>	100GHz (5-10V)						
<i>BTO</i>	Integrated with SiPh/CMOS		Integrated PIC with SiPh	Integrated PIC with CMOS			
<i>Modulator</i>	20-30GHz	30-40GHz	50GHz	70GHz	100GHz		
<i>TFLN</i>	Multi-channel array	Integrated PIC with SiPh	Integrated PIC with CMOS				
<i>Modulator</i>	50GHz (3-8V)	70GHz (2-5V)	90GHz (2-5V)	100GHz			
PASSIVE PLATFORM							
<i>Silicon Photonics</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source	30-40GHz	50GHz	70GHz	80GHz		
<i>WG/SSC/Mux/Coupler</i>	PIC w/Mux/SSC/PD/GC + LD source	30-40GHz	50GHz	70GHz	100GHz	120GHz	
<i>Dielectric/Glass/Silica</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source	30-40GHz	50GHz	70GHz	100GHz	120GHz	
<i>WG/SSC/Mux/Coupler</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source	30-40GHz	50GHz	70GHz	100GHz	120GHz	
<i>InP</i>	Integrated PCB/Interposer w/Mux/SSC/PD/GC + LD source	30-40GHz	50GHz	70GHz	80GHz	90GHz	
<i>Polymer</i>	PCB/Interposer w/Mux/SSC/PD/GC + LD source	30-40GHz	50GHz	70GHz	80GHz	90GHz	

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Hybrid PIC roadmap - datacom

	2026	2028	2030....
1600Gbps	Purple Brick Wall	3200Gbps	6.4Tbps
10Tbps/1U		100Tbps/1U	Purple Brick Wall
30/CP	OSFP/OBO/CP	Purple Brick Wall	Micro-OSFP/OBO/CP
<2km		<2km	<2km
5/Gbps	Purple Brick Wall	\$0.25/Gbps	<\$0.1/Gbps
<\$1/Gbps	Purple Brick Wall	<\$0.5/Gbps	<\$0.2/Gbps
100m		1-100m	
25/Gbps	Purple Brick Wall	<\$0.1/Gbps	<\$0.05/Gbps
<\$0.5/Gbps	Purple Brick Wall	\$0.25/Gbps	<\$0.15/Gbps
		Micro Ring resonator	Micro Ring resonator



Hybrid PIC roadmap - datacom

2022 Roadmap	2022	2024	2026	2028	2030.....2040	
Modules/TxRx Data rate density Form factor	800Gbps 25 Tbps/1U Q/OSFP	1600Gbps 50Tbps/1U OSFP/OBO/CP	Purple Brick Wall 100Tbps/1U OSFP/OBO/CP	3200Gbps 6.4Tbps Purple Brick Wall 400Tbps/1U Purple Brick Wall Micro-OSFP/OBO/CP	12.8Tbps 25.2Tbps 800Tbps/1U	50.4Tbps
Typical link reach Ind wish (@800Gbps) Industry plan	<10km <\$1/Gbps	<10km \$0.5/Gbps	<2km <\$1/Gbps Purple Brick Wall	<2km \$0.25/Gbps Purple Brick Wall	<2km <\$0.1/Gbps Purple Brick Wall	<2km <\$0.1/Gbps
Typical link reach Ind wish (@800Gbps) Industry plan	10-100m <\$0.5/Gbps \$1-3/Gbps	5-100m <\$0.25/Gbps <\$1/Gbps	5-100m <\$0.5/Gbps Purple Brick Wall	1-100m <\$0.1/Gbps \$0.25/Gbps	1-100m <\$0.05/Gbps <\$0.15/Gbps	
ACTIVE PLATFORM						
<i>Silicon Photonics</i>	TW carrier inj 25-35GHz (4-6V)	TW carrier inj 35GHz (3-6V)	Micro Ring resonator 50GHz (2-6V)	Micro Ring resonator 70GHz (2-6V)		
<i>Indium Phosphide</i>	PIC DD/Coherent 30-40GHz (1-4V)	DFB/DBR/SOA 35-50GHz (1-5V)	OEIC Tx/Rx DD/Coh with MSI 60GHz (2-8V)	OEIC Tx/Rx DD/Coh with MSI 80GHz (3-10V)	OEIC Tx/Rx DD/Coh with LSI	
<i>EO Polymer</i>	Slot waveguide 70GHz (<1V)	Integrated PIC 100GHz (<0.5V)	slot w/G 110GHz (<0.5V)	Purple Brick Wall	150GHz (<1V)	
<i>Metal/plasmonic</i>	Slot L/E PIC 100GHz (5-10V)	Coh/DD slot L/E PIC 150GHz (3-8V)	1310/1550nm 200GHz (1-5V)	Purple Brick Wall	300GHz (1-3V)	
<i>BTO</i>	Integrated with SiPh/CMOS 20-30GHz	Integrated PIC with CMOS 30-40GHz	Purple Brick Wall	50GHz	70GHz	
<i>TFLN</i>	Multi-channel array 50GHz (3-8V)	Integrated PIC with SiPh 70GHz (2-5V)	Integrated PIC with CMOS 90GHz (2-5V)	Purple Brick Wall	100GHz	
PASSIVE PLATFORM						
<i>Silicon Photonics</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	Purple Brick Wall	70GHz	80GHz	
<i>Dielectric/Glass/Silica</i>	PIC w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	70GHz	Purple Brick Wall	100GHz	
<i>InP</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	70GHz	Purple Brick Wall	100GHz	
<i>Polymer</i>	PCB/Interposer w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	70GHz	Purple Brick Wall	80GHz	

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Hybrid PIC roadmap - datacom

2022 Roadmap	2022	2024	2026	2028	2030.....2040	
Modules/TxRx Data rate density Form factor	800Gbps 25 Tbps/1U Q/OSFP	1600Gbps 50Tbps/1U OSFP/OBO/CP	Purple Brick Wall 100Tbps/1U OSFP/OBO/CP	3200Gbps 6.4Tbps Purple Brick Wall 400Tbps/1U Purple Brick Wall Micro-OSFP/OBO/CP	12.8Tbps 25.2Tbps 800Tbps/1U	50.4Tbps
Typical link reach Ind wish (@800Gbps) Industry plan	<10km <\$1/Gbps	<10km \$0.5/Gbps	<2km Purple Brick Wall <\$1/Gbps	<2km \$0.25/Gbps Purple Brick Wall <\$0.5/Gbps	<2km <\$0.1/Gbps Purple Brick Wall <\$0.2/Gbps	<2km <\$0.1/Gbps
Typical link reach Ind wish (@800Gbps) Industry plan	10-100m <\$0.5/Gbps \$1-3/Gbps	5-100m <\$0.25/Gbps <\$1/Gbps	Purple Brick Wall <\$0.5/Gbps	Purple Brick Wall <\$0.1/Gbps \$0.25/Gbps	1-100m <\$0.05/Gbps <\$0.15/Gbps	
ACTIVE PLATFORM						
<i>Silicon Photonics</i>	TW carrier inj 25-35GHz (4-6V)	TW carrier inj 35GHz (3-6V)	Micro Ring resonator 50GHz (2-6V)	Purple Brick Wall	Micro Ring resonator 70GHz (2-6V)	
<i>Indium Phosphide</i>	PIC DD/Coherent 30-40GHz (1-4V)	DFB/DBR/SOA 35-50GHz (1-5V)	OEIC Tx/Rx DD/Coh with MSI 60GHz (2-8V)	Purple Brick Wall	OEIC Tx/Rx DD/Coh with MSI 80GHz (3-10V)	
<i>EO Polymer</i>	Slot waveguide 70GHz (<1V)	Integrated PIC 100GHz (<0.5V)	slot W/G 110GHz (<0.5V)	Purple Brick Wall	150GHz (<1V)	170GHz
<i>Metal/plasmonic EO polymer</i>	Slot L/E PIC 100GHz (5-10V)	150GHz (3-8V)	Coh/DD slot L/E PIC 200GHz (1-5V)	Purple Brick Wall	300GHz (1-3V)	400GHz
<i>BTO</i>	Integrated with SiPh/CMOS 20-30GHz	30-40GHz	Integrated PIC with CMOS 50GHz	Purple Brick Wall	70GHz	
<i>TFLN</i>	Multi-channel array 50GHz (3-8V)	Integrated PIC with SiPh 70GHz (2-5V)	Integrated PIC with CMOS 90GHz (2-5V)	Purple Brick Wall	100GHz	
PASSIVE PLATFORM						
<i>Silicon Photonics</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	Purple Brick Wall	70GHz	80GHz	
<i>Dielectric/Glass/Silica</i>	PIC w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	Purple Brick Wall	70GHz	120GHz	
<i>InP</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	70GHz	Purple Brick Wall	100GHz	120GHz
<i>Polymer</i>	PCB/Interposer w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	70GHz	Purple Brick Wall	80GHz	90GHz

Enlarged next slide

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Hybrid PIC roadmap - datacom

2022 Roadmap	2022	2024	2026	2028	2030.....2040			
Modules/TxRx	800Gbps	1600Gbps	Purple Brick Wall	3200Gbps	6.4Tbps	12.8Tbps	25.2Tbps	50.4Tbps
Data rate density	25 Tbps/1U	50Tbps/1U	100Tbps/1U	Purple Brick Wall	400Tbps/1U	800Tbps/1U		
Form factor	Q/OSFP	OSFP/OBO/CP	OSFP/OBO/CP	Purple Brick Wall	Micro-OSFP/OBO/CP			
Typical link reach	<10km	<10km	<2km	Purple Brick Wall	<2km			
Ind wish (@800Gbps)	<\$1/Gbps	\$0.5/Gbps	Purple Brick Wall	\$0.25/Gbps				

ACTIVE PLATFORM	2022	2024	2026	2028	2030.....2040
Silicon Photonics Modulator	TW carrier inj 25-35GHz (4-6V)	TW carrier inj 35GHz (3-6V)	Micro Ring resonator 50GHz (2-6V)	Purple Brick Wall	Micro Ring resonator 70GHz (2-6V)
Indium Phosphide Laser/Modulator	PIC DD/Coherent DFB/DBR/SOA 30-40GHz (1-4V)	1310/1550nm 35-50GHz (1-5V)	OEIC Tx/Rx DD/Coh with MSI 60GHz (2-8V)	Purple Brick Wall	80GHz (3-10V) OEIC Tx/Rx DD/Coh with LSI
EO Polymer Modulator	Slot waveguide 70GHz (<1V)	1310/1550nm Integrated PIC slot W/G 100GHz (<0.5V)	110GHz (<0.5V)	Purple Brick Wall	150GHz (<1V)
Metal/plasmonic EO polymer Modulator	Slot L/E PIC 100GHz (5-10V)	1310/1550nm 150GHz (3-8V)	Coh/DD slot L/E PIC 30-40GHz	200GHz (1-5V)	Purple Brick Wall 300GHz (1-3V)
BTO Modulator	Integrated with SiPh/CMOS 20-30GHz	Integrated PIC with CMOS 30-40GHz	Purple Brick Wall	50GHz	70GHz
TFLN Modulator	Multi-channel array 50GHz (3-8V)	Integrated PIC with SiPh 70GHz (2-5V)	Integrated PIC with CMOS 90GHz (2-5V)	Purple Brick Wall	100GHz

PASSIVE PLATFORM	2022	2024	2026	2028	2030.....2040
Silicon Photonics WG/SSC/Mux/Coupler	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	Purple Brick Wall	70GHz	80GHz
Dielectric/Glass/Silica WG/SSC/Mux/Coupler	PIC w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	70GHz	Purple Brick Wall	100GHz 120GHz
InP WG/SSC/Mux/Coupler	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	70GHz	Purple Brick Wall	100GHz 120GHz
Polymer WG/SSC/Mux/Coupler	Integrated PCB/Interposer w/Mux/SSC/PD/GC + LD source 30-40GHz	50GHz	70GHz	Purple Brick Wall	80GHz 90GHz

Normal Black Font = Reasonably expected based on current efforts	Purple Brick Wall = Technology cost barrier	Slanted Red Font = Major industry effort required for commercialization
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Draft Roadmap 2022 (NEW)

Warning - Eye-chart!

Don't try and read it – zoom soon

(can be found at www.lightwavelogic.com)



Hybrid PIC roadmap - datacom

2022 Roadmap	2022	2024	2026	2028	2030.....2040	
Modules/TxRx Data rate density Form factor	800Gbps 25 Tbps/1U Q/OSFP	1600Gbps 50Tbps/1U OSFP/OBO/CP	Purple Brick Wall 100Tbps/1U OSFP/OBO/CP	3200Gbps 6.4Tbps Purple Brick Wall 400Tbps/1U Purple Brick Wall Micro-OSFP/OBO/CP	12.8Tbps 25.2Tbps 800Tbps/1U	50.4Tbps
Typical link reach Ind wish (@800Gbps) Industry plan	<10km <\$1/Gbps	<10km \$0.5/Gbps	<2km Purple Brick Wall \$0.25/Gbps	<2km Purple Brick Wall \$0.25/Gbps	<2km <\$0.1/Gbps <\$0.2/Gbps	<2km <\$0.1/Gbps
Typical link reach Ind wish (@800Gbps) Industry plan	10-100m <\$0.5/Gbps \$1-3/Gbps	5-100m <\$0.25/Gbps <\$1/Gbps	Purple Brick Wall <\$0.5/Gbps	Purple Brick Wall <\$0.1/Gbps \$0.25/Gbps	1-100m <\$0.05/Gbps <\$0.15/Gbps	
ACTIVE PLATFORM						
<i>Silicon Photonics</i>	TW carrier inj	TW carrier inj	Micro Ring resonator	Micro Ring resonator		
<i>Modulator</i>	25-35GHz (4-6V)	35GHz (3-6V)	50GHz (2-6V)	70GHz (2-6V)		
<i>Indium Phosphide</i>	PIC DD/Coherent	DFB/DBR/SOA	1310/1550nm	OEIC Tx/Rx DD/Coh with MSI	OEIC Tx/Rx DD/Coh with LSI	
<i>Laser/Modulator</i>	30-40GHz (1-4V)	35-50GHz (1-5V)	50GHz (2-8V)	Purple Brick Wall	80GHz (3-10V)	
<i>EO Polymer</i>	Slot waveguide	1310/1550nm	Integrated PIC slot W/G	1310/1550nm		
<i>Modulator</i>	70GHz (<1V)	100GHz (<0.5V)	110GHz (<0.5)	Purple Brick Wall	150GHz (<1V)	
<i>Metal/plasmonic EO polymer</i>	Slot L/E PIC	1310/1550nm	Coh/DD slot L/E PIC	1310/1550nm		
<i>Modulator</i>	100GHz (5-10V)	150GHz (3-8V)	200GHz (1-5V)	Purple Brick Wall	300GHz (1-3V)	
<i>BTO</i>	Integrated with SiPh/CMOS	Integrated PIC with CMOS				
<i>Modulator</i>	20-30GHz	30-40GHz	Purple Brick Wall	50GHz	70GHz	
<i>TFLN</i>	Multi-channel array	Integrated PIC with SiPh	Integrated PIC with CMOS			
<i>Modulator</i>	50GHz (3-8V)	70GHz (2-5V)	90GHz (2-5V)	Purple Brick Wall	100GHz	
PASSIVE PLATFORM						
<i>Silicon Photonics</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source	50GHz	Purple Brick Wall	SSI OEIC IC+SiPh w/LD/MRR	MSI OEIC IC+SiPh + LD/MRR	
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	70GHz	80GHz	
<i>Dielectric/Glass/Silica</i>	PIC w/Mux/SSC/PD/GC + LD source			SSI PIC with SiPh w/LD/Hybrid modulator	MSI PIC with SiPh w/LD/Hybrid modulator	
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	Purple Brick Wall	100GHz	
<i>InP</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source			SSI OEIC w/Hybrid modulator	MSI OEIC w/Hybrid modulator	
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	Purple Brick Wall	100GHz	
<i>Polymer</i>	Integrated PCB/Interposer w/Mux/SSC/PD/GC + LD source			PCB/Interposer w/Mux/SSC/PD/GC w/LD/Hybrid modulator		
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	Purple Brick Wall	80GHz	

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Hybrid PIC roadmap - datacom

2022 Roadmap	2022	2024	2026	2028	2030.....2040	
Modules/TxRx Data rate density Form factor	800Gbps 25 Tbps/1U Q/OSFP	1600Gbps 50Tbps/1U OSFP/OBO/CP	Purple Brick Wall 100Tbps/1U OSFP/OBO/CP	3200Gbps 6.4Tbps 400Tbps/1U Micro-OSFP/OBO/CP	12.8Tbps 25.2Tbps 800Tbps/1U	50.4Tbps
Typical link reach Ind wish (@800Gbps) Industry plan	<10km <\$1/Gbps	<10km \$0.5/Gbps	<2km \$0.25/Gbps	<2km \$0.1/Gbps	<2km <\$0.1/Gbps	<2km <\$0.1/Gbps
Typical link reach Ind wish (@800Gbps) Industry plan	10-100m <\$0.5/Gbps	5-100m <\$0.25/Gbps	Purple Brick Wall <\$0.1/Gbps	1-100m \$0.25/Gbps	<\$0.05/Gbps	<\$0.15/Gbps
ACTIVE PLATFORM						
<i>Silicon Photonics</i>	TW carrier inj	TW carrier inj	Micro Ring resonator	Micro Ring resonator		
<i>Modulator</i>	25-35GHz (4-6V)	35GHz (3-6V)	50GHz (2-6V)	70GHz (2-6V)		
<i>Indium Phosphide</i>	PIC DD/Coherent	DFB/DBR/SOA	1310/1550nm	OEIC Tx/Rx DD/Coh with MSI	OEIC Tx/Rx DD/Coh	
<i>Laser/Modulator</i>	30-40GHz (1-4V)	35-50GHz (1-5V)	50GHz (2-8V)	80GHz (3-10V)		
<i>EO Polymer</i>	Slot waveguide	1310/1550nm	Integrated PIC slot W/G	1310/1550nm		
<i>Modulator</i>	70GHz (<1V)	100GHz (<0.5V)	110GHz (<0.5)	150GHz		
<i>Metal/plasmonic EO polymer</i>	Slot L/E PIC	1310/1550nm	Coh/DD slot L/E PIC	1310/1550nm		
<i>Modulator</i>	100GHz (5-10V)	150GHz (3-8V)	200GHz (1-5V)	300GHz		
<i>BTO</i>	Integrated with SiPh/CMOS	Integrated PIC with CMOS				
<i>Modulator</i>	20-30GHz	30-40GHz	50GHz	70GHz		
<i>TFLN</i>	Multi-channel array	Integrated PIC with SiPh	Integrated PIC with CMOS			
<i>Modulator</i>	50GHz (3-8V)	70GHz (2-5V)	90GHz (2-5V)	100GHz		
PASSIVE PLATFORM						
<i>Silicon Photonics</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source	50GHz	70GHz	SSI OEIC IC+SiPh w/LD/MRR	MSI OEIC IC+SiPh	
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	100GHz	120GHz	
<i>Dielectric/Glass/Silica</i>	PIC w/Mux/SSC/PD/GC + LD source		SSI PIC with SiPh w/LD/Hybrid modulator		MSI PIC with SiPh w/LD/Hybrid modulator	
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	100GHz	120GHz	
<i>InP</i>	Coherent/DD PIC w/Mux/SSC/PD/GC + LD source		SSI OEIC w/Hybrid modulator		MSI OEIC w/Hybrid modulator	
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	100GHz	120GHz	
<i>Polymer</i>	Integrated PCB/Interposer w/Mux/SSC/PD/GC + LD source		PCB/Interposer w/Mux/SSC/PD/GC w/LD/Hybrid modulator			
<i>WG/SSC/Mux/Coupler</i>	30-40GHz	50GHz	70GHz	80GHz	90GHz	

Purple region shows trends of the 'purple brick wall' areas that need to be addressed seriously

Normal Black Font = Reasonably expected based on current efforts	Purple Brick Wall = Technology cost barrier	Slanted Red Font = Major industry effort required for commercialization
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A server room with rows of black server racks. The room is dimly lit, with glowing blue and orange light trails swirling through the air, suggesting data flow or network activity. The text "Observations... For debate..." is overlaid in the center in a white, sans-serif font.

Observations...
For debate...

Observations and *controversial* topics...



LIGHTWAVE

2022 Roadmap	2022	2024	2026	2028	2030.....2040
Modules/TxRx Data rate density Form factor	800Gbps 25 Tbps/1U Q/OSFP	1600Gbps 50Tbps/1U OSFP/OBO/CP	Purple Brick Wall 100Tbps/1U OSFP/OBO/CP	3200Gbps 6.4Tbps Purple Brick Wall 400Tbps Micro	12.8Tbps Purple Brick Wall 1U 50.4Tbps
Typical link reach Ind wish (@800Gbps) Industry plan	<10km <\$1/Gbps	<10km \$0.5/Gbps	<2km Purple Brick Wall	<2km \$0.25/Gbps	<2km \$1/Gbps <\$0.1/Gbps
Typical link reach Ind wish (@800Gbps) Industry plan	10-100m <\$0.5/Gbps	5-100m <\$0.25/Gbps	Purple Brick Wall	1-100m <\$0.1/Gbps	1-100m \$0.25/Gbps
ACTIVE PLATFORM					
<i>Silicon Photonics</i>	TW carrier inj	TW carrier inj	Micro Ring resonator	Micro Ring resonator	
<i>Indium Phosphide</i>	25-35GHz (4-6V)	35GHz (3-6V)	50GHz (2-6V)	70GHz (2-6V)	
<i>EO Polymer</i>	PIC DD/Coherent	DFB/DBR/SOA	1310/1550nm	OEIC Tx/Rx DD/Coh with MSI	OEIC Tx/Rx DD/Coh with LSI
<i>Metal/plasmonic</i>	30-40GHz (1-4V)	35-50GHz (1-5V)	50GHz (2-8V)	80GHz (3-10V)	
<i>BTO</i>	slot waveguide	1310/1550nm	110GHz (<0.5)	150GHz (<1)	170GHz
<i>TFLN</i>	slot L/E PIC	1310/1550nm	200GHz (1-5V)	300GHz (1-5V)	
<i>Si</i>	integrated with SiPh/CMOS	integrated PIC with CMOS	integrated PIC with CMOS	integrated PIC with CMOS	
<i>SiN</i>	20-30GHz	20-30GHz	50GHz	70GHz	100GHz
<i>SiC</i>	integrated PIC with SiPh	integrated PIC with SiPh	integrated PIC with SiPh	integrated PIC with SiPh	
<i>SiGe</i>	LD source	LD source	LD source	LD source	
<i>Si</i>	70GHz	70GHz	70GHz	70GHz	
<i>SiC</i>	PD/GC + LD source	PD/GC + LD source	PD/GC + LD source	PD/GC + LD source	
<i>Si</i>	70GHz	70GHz	70GHz	70GHz	

Challenge for Tbps transceivers – is this possible?

Challenge for cost per Gbps (@800Gbps) – will we achieve the cost metrics?

Trend for higher integration with a hybrid PIC – are we going to see electronics, and higher integration levels with mix/match technologies?

Hybrid technologies with natural speed/low power – when will they be implemented?

Hybrid modulators – will they be key for PICs this decade?

Purple Brick Wall
Technology cost barrier
Slanted Red Font = Major industry effort required for commercialization

A server room with rows of server racks. The racks are dark with some blue and green lights. In the foreground, there are several glowing, curved light trails in shades of blue, orange, and purple, suggesting data flow or network activity. The ceiling is a standard grid pattern.

Company address

369 Inverness Parkway, Suite 350
Englewood, CO 80112

lightwavelogic.com

Thank you!

A server room with rows of black server racks. The scene is illuminated by vibrant, glowing light trails in shades of blue, orange, and purple that swirl and flow through the aisle. The text "Back up" is centered in a white, bold, sans-serif font.

Back up



Draft PIC package roadmap

2022

Roadmap (PIC)	2021	2022	2024	2026	2028	2030
Packaging						
Modules/TxRx	400Gbps	800Gbps	1600Gbps	3200Gbps	6400Gbps	
Data rate density	25 Tbps/1U		100Tbps/1U	400Tbps/1U	1600Tbps/1U	
Form factor	Q/OSFP	OSFP/OBO/CP	OBO/CP	Co-Pkg/CoB	Micro-Co-Pkg/CoB	
Typical link reach	<10km	<10km	<2km	<2km	<2km	<2km
Ind wish (@800Gbps)	\$2/Gbps	\$1/Gbps	\$0.5/Gbps	\$0.5/Gbps	<\$0.2/Gbps	\$0.2/Gbps
Industry plan	>\$5/Gbps (<2km)	<\$2/Gbps		\$0.5/Gbps		\$0.2/Gbps
Typical link reach	10-100m	5-50m	1-25m	1-25m		
Ind wish (@800Gbps)	<\$1/Gbps	<\$0.5/Gbps	<\$0.25/Gbps	<\$0.05/Gbps		
Industry plan		\$1/Gbps		\$0.25/Gbps		<\$0.15/Gbps
Gold Box	Butterfly	micro-butterfly	nano-butterfly			
50GHz	100GHz	150GHz	200GHz			
Form factor: PIC	chips <10 functions	10-50 functions	100-200 functions	500 functions		
Surface mount	SOIC (<50 lead)	micro-SOIC (<50 lead)	(100+ lead)			
25GHz	50GHz	70GHz (100Gbps NRZ)	100GHz (130Gbps NRZ)			
Connectorized SM/MM fiber	Fiber ribbons 1x12/24	2D fiber ribbons 2x24/48	2D fiber ribbons >500 fibers			
Flip-chip bumping to pcb	<100 bumps	<250 bumps	<1000 bumps			
Thermal passive heat management		advanced thermal designs				
Chip-on-board & wafer-scale	Flip-chip bump (100)	1000 devices	10000 devices	100,000 devices		
Interconnect bandwidth	25GHz	50GHz	70GHz	100GHz	200GHz	
Wafer format	150mm	200mm	300mm	450mm		
Fiber to PIC packaging (grating/edge)	micro-optics to PIC packaging (grating/edge)	terposer to PIC packaging (edge/evanescent)				
2D Integration	2.5D integration	3D integration				
Co-pkg (layer 1 - CoC)	2 chips	10 chips	30 chips	70GHz	150GHz	50 chips
25GHz	50GHz					
2D Integration (electronic IC on PIC)	2.5D integration (electronic IC and PIC on carrier)	PIC on interposer (Optical)	TEC integrated directly PIC			
Active cooling (standard TEC)	Customized TEC/controller	Graphene based materials	Integrated with PIC pkg			
Passive cooling (std heat spreaders)						
Co-pkg (layer 2 - Comp)	10 devices	100 devices	1000 devices			
25GHz	50GHz	70GHz				
Single die	twon die	multiple die 2D	multiple die 3D/fan out interconnect	multiple die 3D/double sided		
Optical platform	150mm	Optical platform 200mm	optical platform 300mm			
Electronic and photonic PIC 2D package	electronic and photonics PIC 2.5D package					
						C 3D package platform

Normal Black Font = Reasonably expected based on current efforts	Purple Brick Wall = Technology cost barrier	Slanted Red Font = Major industry effort required for commercialization
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CoC = Chip-on-Carrier

A PIC Packaging roadmap...trends towards chip scale packaging/Testing-Assembly-Packaging (CSP-TAP)



Draft PIC package roadmap

2022

Roadmap (PIC)	2021	2022	2024	2026	2028	2030
Packaging	400Gbps 25 Tbps/1U Q/OSFP	800Gbps OSFP/OBO/CP	100Tbps/1U OBO/CP	1600Gbps Purple Brick	3200Gbps Co-Pkg/CoB	6400Gbps Micro-Co-Pkg/CoB
Typical link reach Ind wish (@800Gbps) <i>Industry plan</i>	<10km \$2/Gbps	<10km \$1/Gbps	<2km Purple Brick	<2km Purple Brick	<2km Purple Brick	<2km Purple Brick
Typical link reach Ind wish (@800Gbps) <i>Industry plan</i>	10-100m <\$1/Gbps	5-50m <\$0.5/Gbps	<\$0.25/Gbps Purple Brick	1-25m Purple Brick	<\$0.05/Gbps Purple Brick	<\$0.15/Gbps Purple Brick
Gold Box	Butterfly 50GHz Form factor: PIC chips <10 functions	micro-butterfly 100GHz 10-50 functions	150GHz 10-50 functions	nano-butterfly 100-200 functions	200GHz 500 functions	500 functions
Surface mount	SOIC (<50 lead) 25GHz Connectorized SM/MM fiber Flip-chip bumping to pcb <100 bumps Thermal passive heat management	micro-SOIC (<50 lead) 50GHz Fiber ribbons 1x12/24 <100 bumps advanced thermal designs	micro-SOIC (<50 lead) 70GHz (100Gbps NRZ) <250 bumps advanced thermal designs	(100+lead) 2D fiber ribbons 2x24/48 <1000 bumps	100GHz (130Gbps NRZ) 2D fiber ribbons <10,000 bumps	200GHz <10,000 bumps
Chip-on-board & wafer-scale	Flip-chip bump (100) Interconnect bandwidth 25GHz Wafer format 150mm Fiber to PIC packaging (grating/edge) 2D Integration	1000 devices 50GHz 200mm micro-optics to PIC packaging (grating/edge)	10000 devices 70GHz 300mm micro-optics to PIC packaging (grating/edge)	100GHz 300mm 3D integration	100,000 devices 450mm interposer to PIC packaging (edge/evanescent)	200GHz
Co-pkg (layer 1 - CoC)	2 chips 25GHz 2D Integration (electronic IC on PIC) Active cooling (standard TEC) Passive cooling (std heat spreaders)	10 chips 50GHz 2.5D integration (electronic IC and PIC on carrier) Customized TEC/controller	30 chips 70GHz 2.5D integration (electronic IC and PIC on carrier) Graphene based materials.	50 chips 150GHz micro-TEC pkg with PIC Integrated with PIC pkg.	50 chips PIC on interposer (Optical) TEC integrated directly PIC Integrated with PIC	50 chips
Co-pkg (layer 2 - Comp)	10 devices 25GHz Single die Optical platform 150mm Electronic and photonic PIC 2D package	100 devices 50GHz multiple die 2D Optical platform 200mm electronic and photonics PIC 2.5D package	70GHz multiple die 3D/fan out interconnect optical platform 300mm	1000 devices multiple die 3D/double sided optical platform 300mm	1000 devices multiple die 3D/double sided C 3D package platform	C 3D package platform
	Normal Black Font = Reasonably expected based on current efforts		Purple Brick Wall = Technology cost barrier		Slanted Red Font = Major industry effort required for commercialization	

As per the silicon electronics industry Chip scale packaging (CSP-TAP)

CoC = Chip-on-Carrier

A PIC Packaging roadmap... trends towards chip scale packaging/Testing-Assembly-Packaging (CSP-TAP)